

16-bit Proprietary Microcontroller

CMOS

F²MC-16L MB90670/675 Series

MB90671/672/673/T673/P673 (MB90670 Series) MB90676/677/678/T678/P678 (MB90675 Series)

■ DESCRIPTION

The MB90670/675 series is a member of 16-bit proprietary single-chip microcontroller F²MC*1-16L family designed to be combined with an ASIC (Application Specific IC) core. The MB90670/675 series is a high-performance general-purpose 16-bit microcontroller for high-speed real-time processing in various industrial equipment, OA equipment, and process control.

The instruction set of F²MC-16L CPU core inherits AT architecture of F²MC-8 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data (32-bit).

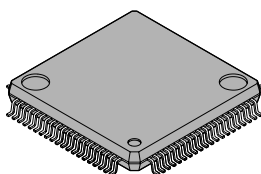
The MB90670/675 series has peripheral resources of UART0, UART1(SCI), an 8/10-bit A/D converter, an 8/16-bit PPG timer, a 16-bit reload timer, a 24-bit free-run timer, an output compare (OCU), an input capture (ICU), DTP/external interrupt circuit, an I²C*2 interface (in MB90675 series only). Embedded peripheral resources performs data transmission with an intelligent I/O service function without the intervention of the CPU, enabling real-time control in various applications.

*1: F²MC stands for FUJITSU Flexible Microcontroller.

*2: Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

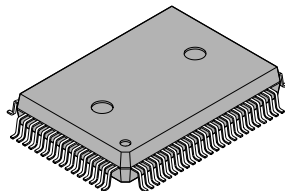
■ PACKAGE

80-pin Plastic LQFP



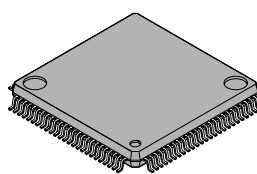
(FPT-80P-M05)

80-pin Plastic QFP



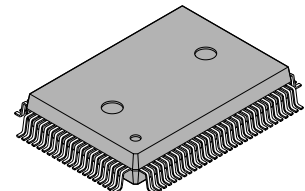
(FPT-80P-M06)

100-pin Plastic LQFP



(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

MB90670/675 Series

■ FEATURES

- Clock
 - Embedded PLL clock multiplication circuit
 - Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).
 - Minimum instruction execution time of 62.5 ns (at oscillation of 4 MHz, four times the PLL clock, operation at V_{cc} of 5.0 V)
- CPU addressing space of 16 Mbytes
 - Internal addressing of 24-bit
 - External accessing can be performed by selecting 8/16-bit bus width (external bus mode)
- Instruction set optimized for controller applications
 - Rich data types (bit, byte, word, long word)
 - Rich addressing mode (23 types)
 - High code efficiency
 - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C) and multi-task operations
 - Adoption of system stack pointer
 - Enhanced pointer indirect instructions
 - Barrel shift instructions
- Enhanced execution speed
 - 4-byte instruction queue
- Enhanced interrupt function
 - 8 levels, 32 factors
- Automatic data transmission function independent of CPU operation
 - Extended intelligent I/O service function (EI²OS)
- Low-power consumption (standby) mode
 - Sleep mode (mode in which CPU operating clock is stopped)
 - Timebase timer mode (mode in which other than oscillation and timebase timer are stopped)
 - Stop mode (mode in which oscillation is stopped)
 - CPU intermittent operation mode
 - Hardware standby mode
- Process
 - CMOS technology
- I/O port
 - MB90670 series: Maximum of 65 ports
 - MB90675 series: Maximum of 84 ports
- Timer
 - Timebase timer/watchdog timer: 1 channel
 - 8/16-bit PPG timer: 8-bit × 2 channels or 16-bit × 1 channel
 - 16-bit reload timer: 2 channels
 - 24-bit free-run timer: 1 channel
- Input capture (ICU)
 - Generates an interrupt request by latching a 24-bit free-run timer counter value upon detection of an edge input to the pin.
- Output compare (OCU)
 - Generates an interrupt request and reverse the output level upon detection of a match between the 24-bit free-run timer counter value and the compare setting value.
- I²C interface (in MB90675 series only)
 - Serial I/O port for supporting Inter IC BUS

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- UART0
With full-duplex double buffer (8-bit length)
Clock asynchronous or clock synchronized transmission (with start and stop bits) can be selectively used.
- UART1 (SCI)
With full-duplex double buffer (8-bit length)
Clock asynchronous or clock synchronized serial transmission (I/O extended serial) can be selectively used.
- DTP/external interrupt circuit (4 channels)
A module for starting extended intelligent I/O service (EI²OS) and generating an external interrupt triggered by an external input.
- Wake-up interrupt
Receives external interrupt requests and generates an interrupt request upon an “L” level input.
- Delayed interrupt generation module
Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
8-bit or 10-bit resolution can be selectively used.
Starting by an external trigger input.

MB90670/675 Series

■ PRODUCT LINEUP

• MB90670 series

Part number	MB90671	MB90672	MB90673	MB90T673	MB90P673
Classification	Mask ROM products			External ROM product	One-time PROM product
ROM size	16 Kbytes	32 Kbytes	48 Kbytes	External ROM	48 Kbytes
RAM size	640 bytes	1.64 Kbytes	2 Kbytes		
CPU functions	Number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock of 16 MHz) Interrupt processing time: 1.5 μ s (at machine clock of 16 MHz, minimum value)				
Ports	General-purpose I/O ports (CMOS output): 57 General-purpose I/O ports (N-ch open-drain output): 8 Total: 65				
UART0	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronous transmission (4800 Kbps to 500 kbps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.				
UART1 (SCI)	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronous transmission (2400 Kbps to 62500 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.				
8/10-bit A/D converter	Conversion precision: 10-bit or 8-bit selectable Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)				
8/16-bit PPG timer	Number of channels: 2 8-bit or 16-bit PPG operation A pulse wave of given intervals and given duty ratios can be output. Pulse cycle: 125 ns to 16.78 s (at oscillation of 4 MHz, machine clock of 16 MHz)				
16-bit reload timer	Number of channels: 2 16-bit reload timer operation Interval: 125 ns to 131 ms (at machine clock of 16 MHz) External event count can be performed.				
24-bit free-run timer	Number of channel :1 Overflow interrupts or intermediate bit interrupts may be generated.				
Output compare unit (OCU)	Number of channels: 8 Pin input factor: A match signal of compare register				

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MB90670/675 Series

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Part number	MB90671	MB90672	MB90673	MB90T673	MB90P673
Item					
Input capture unit (ICU)	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)				
DTP/external interrupt circuit	Number of inputs: 4 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input. External interrupt circuit or extended intelligent I/O service (EI ² OS) can be used.				
Wake-up interrupt	Number of inputs: 8 Started by an "L" level input.				
Delayed interrupt generation module	An interrupt generation module for switching tasks used in real-time operating systems.				
I ² C interface	None				
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)				
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)				
Low-power consumption (standby) mode	Sleep/stop/CPU intermittent operation/timebase timer/hardware stand-by				
Process	CMOS				
Operating voltage*	2.7 V to 5.5 V				

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

MB90670/675 Series

• MB90675 series

Part number	MB90676	MB90677	MB90678	MB90T678	MB90P678	MB90V670
Item						
Classification	Mask ROM products			External ROM product	One-time PROM product	Evaluation product
ROM size	32 Kbytes	48 Kbytes	64 Kbytes	None	64 Kbytes	—
RAM size	1.64 Kbytes	2 Kbytes	3 Kbytes			4 Kbytes
CPU functions	The number of instructions: 340 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock of 16 MHz) Interrupt processing time: 1.5 μ s (at machine clock of 16 MHz, minimum value)					
Ports	General-purpose I/O ports (CMOS output): 74 General-purpose I/O ports (N-ch open-drain output): 10 Total: 84					
UART0	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronous transmission (4800 Kbps to 500 Kbps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.					
UART1 (SCI)	Clock synchronized transmission (500 Kbps to 2 Mbps) Clock asynchronous transmission (2400 Kbps to 62500 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.					
8/10-bit A/D converter	Conversion precision: 10-bit or 8-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel only once) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)					
8/16-bit PPG timer	Number of channels: 2 PPG operation of 8-bit or 16-bit Pulse of given intervals and given duty ratios can be output Pulse interval 125 ns to 16.78 s (at oscillation of 4 MHz, machine clock of 16 MHz)					
16-bit reload timer	Number of channels: 2 16-bit reload timer operation Interval: 125 ns to 131 ms (at machine clock of 16 MHz) External event count can be performed.					
24-bit free-run timer	Number of channel :1 Overflow interrupts or intermediate bit interrupts may be generated.					
Output compare (OCU)	Number of channels: 8 Pin input factor: a match signal of compare register					

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MB90670/675 Series

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Part number Item	MB90676	MB90677	MB90678	MB90T678	MB90P678	MB90V670
Input capture (ICU)	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)					
DTP/external interrupt circuit	Number of inputs: 4 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input. External interrupt circuit or extended intelligent I/O service (EI ² OS) can be used.					
Wake-up interrupt	Number of inputs: 8 Started by an "L" level input.					
Delayed interrupt generation module	An interrupt generation module for switching tasks used in real-time operating systems.					
I ² C interface	Serial I/O port for supporting Inter IC BUS					
Timebase timer	18-bit counter Interrupt interval: 1.024 ms, 4.096 ms, 16.384 ms, 131.072 ms (at oscillation of 4 MHz)					
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)					
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/timebase timer/hardware stand-by					
Process	CMOS					
Power supply voltage for operation*	2.7 V to 5.5 V					

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.") Assurance for the MB90V670 is given only for operation with a tool at a power voltage of 2.7 V to 5.5 V, an operating temperature of 0°C to 70°C, and an operating frequency of 1.5 MHz to 16 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90671 MB90672 MB90673 MB90T673	MB90P673	MB90676 MB90677 MB90678 MB90T678	MB90P678	MB90V670
FPT-80P-M05	○	○	×	×	×
FPT-80P-M06	○	○	×	×	×
FPT-100P-M05	×	×	○	○	×
FPT-100P-M06	×	×	○	○	×

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

MB90670/675 Series

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

In evaluation with an evaluation product, note the difference between the evaluation chip and the chip actually used. The following items must be taken into consideration.

- The MB90V670 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V670, images from FF4400_H to FFFFFFF_H are mapped to bank 00, and FE0000_H to FF3FFF_H to mapped to bank FE and FF only. (This setting can be changed by configuring the development tool.)
- In the MB90678/MB90P678, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FF0000_H to FF3FFF_H to bank FF only.

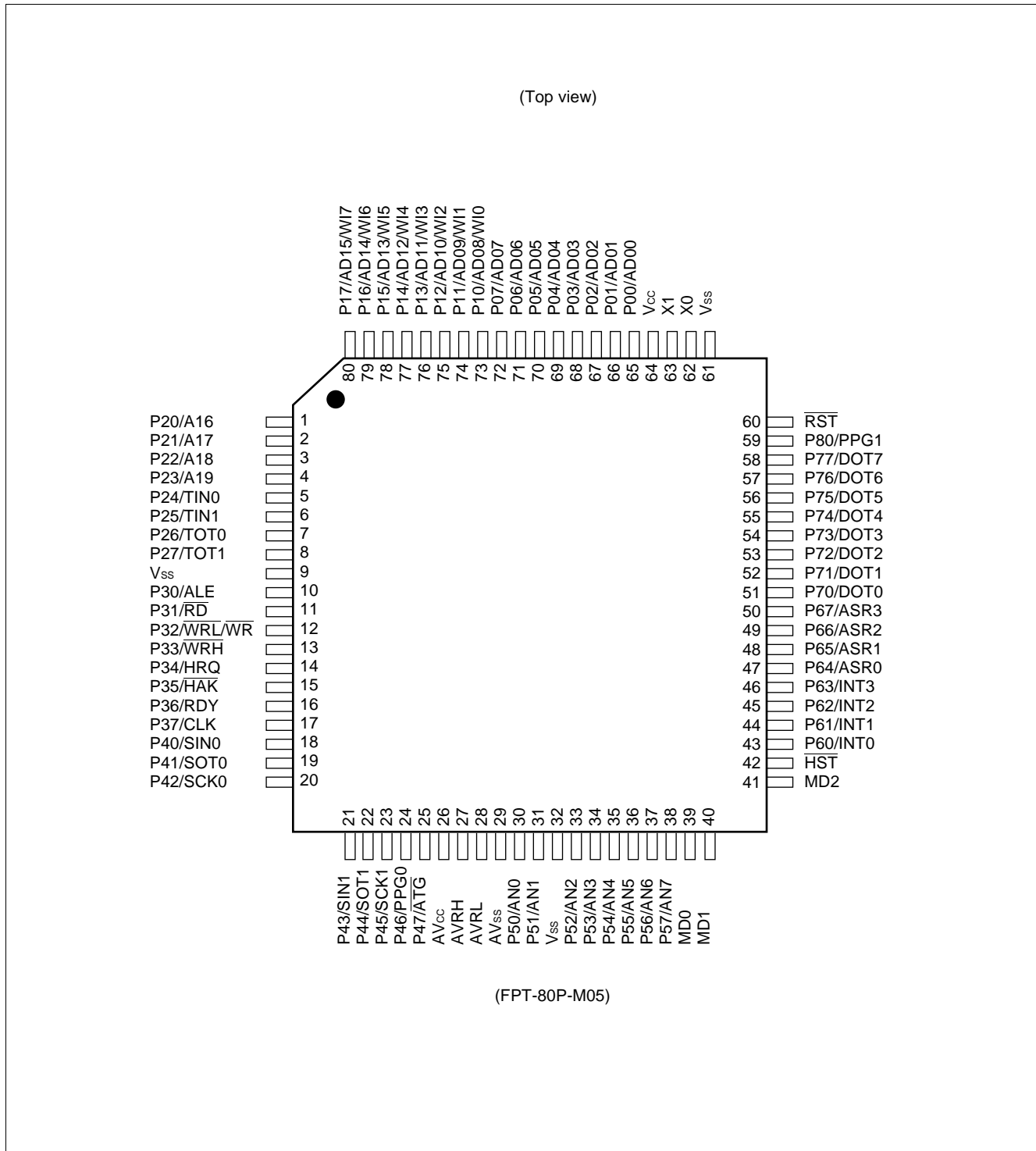
2. Mask Options

Functions selected by optional settings and methods for setting the options are dependent on the product types.

Refer to “■ Mask Options” for detailed information.

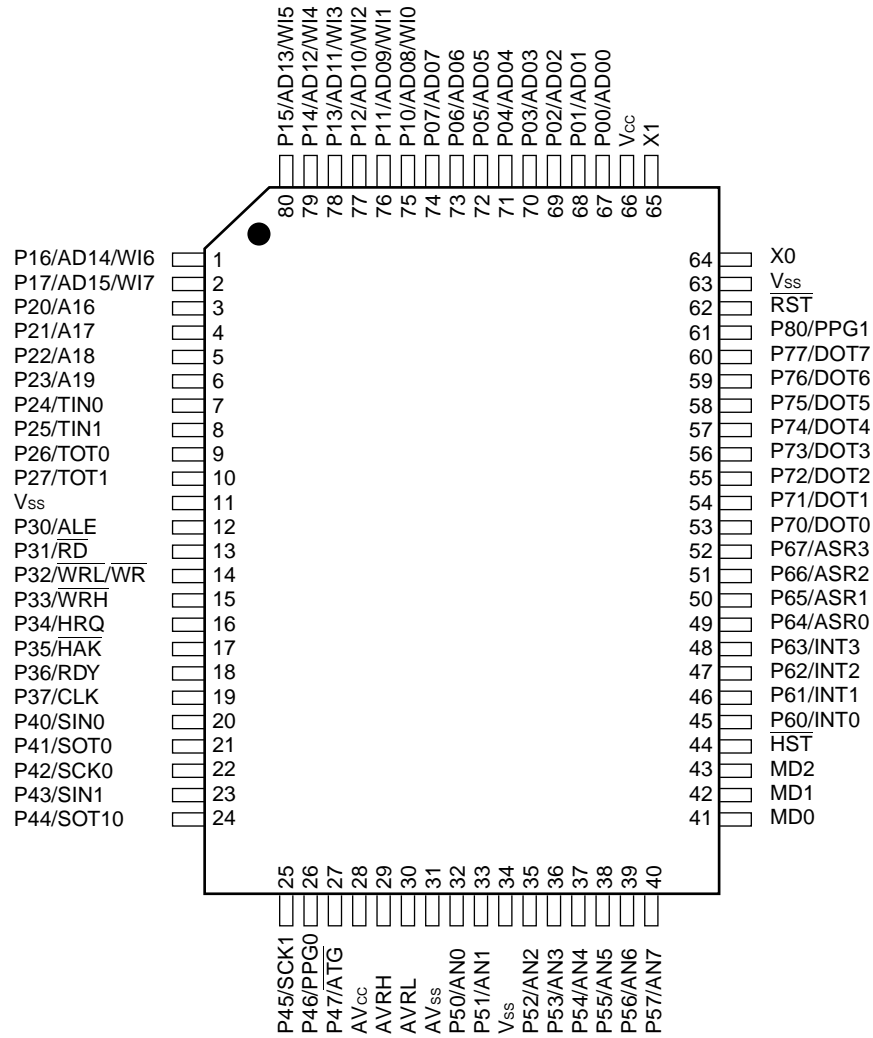
Note that mask option is fixed in MB90V670 series.

■ PIN ASSIGNMENT



MB90670/675 Series

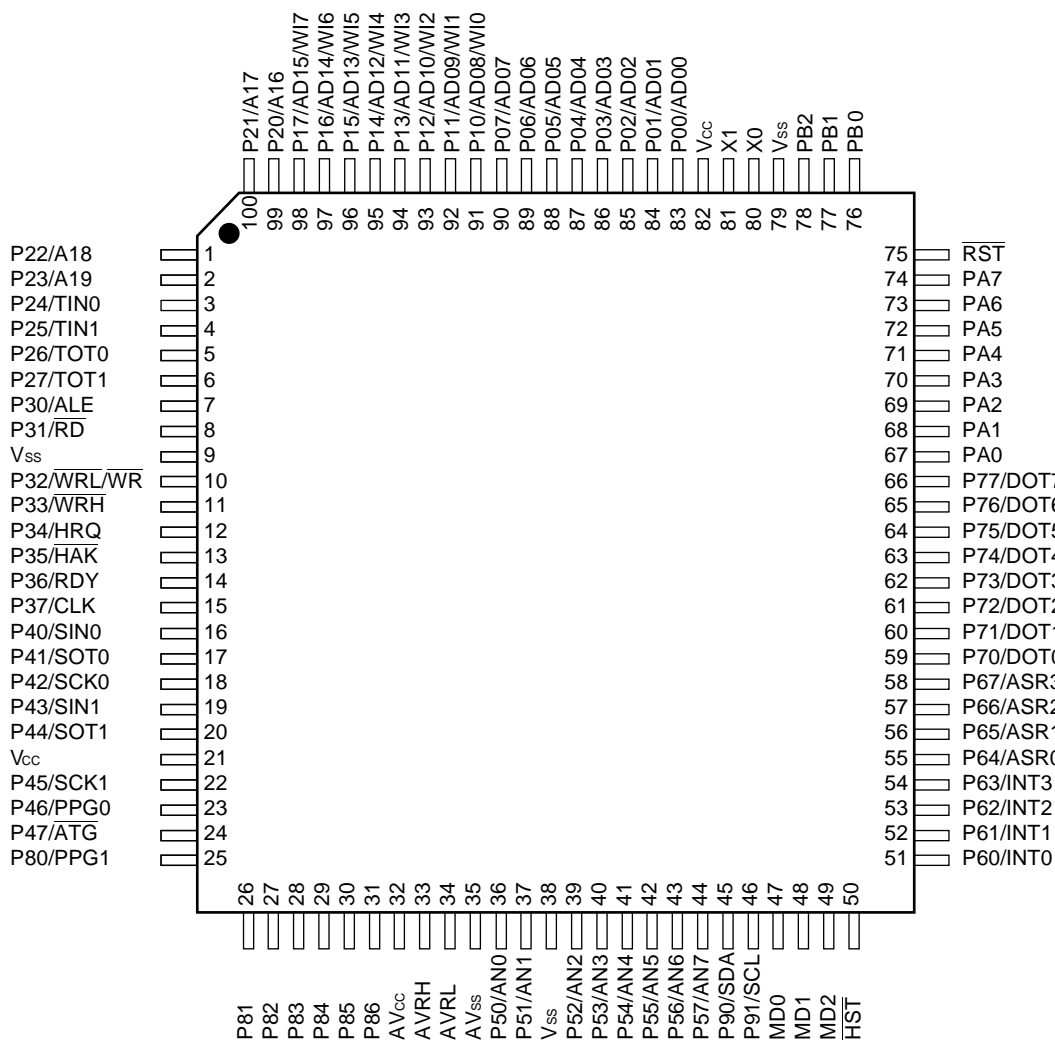
(Top view)



(FPT-80P-M06)

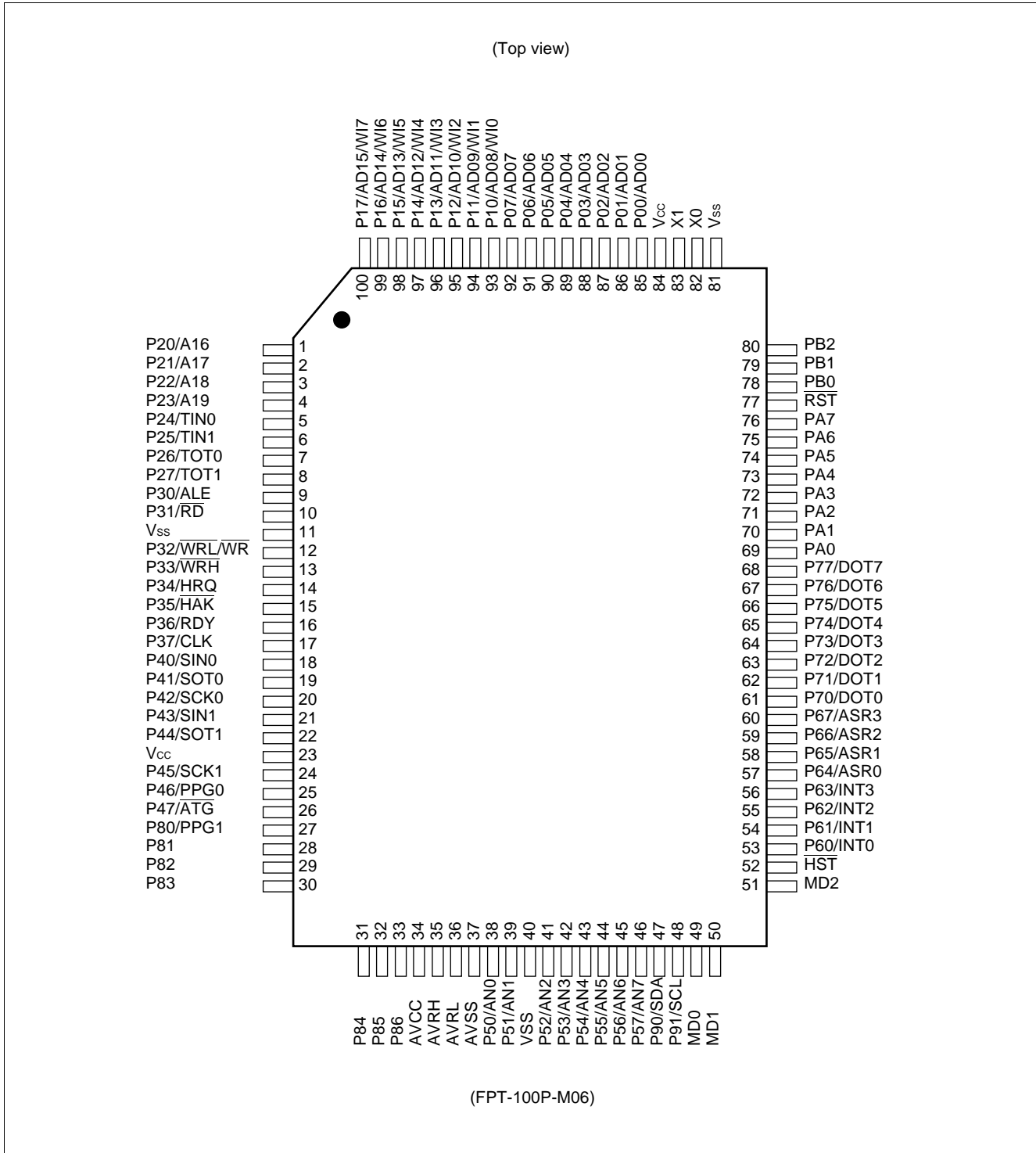
MB90670/675 Series

(Top view)



(FPT-100P-M05)

MB90670/675 Series



MB90670/675 Series

■ PIN DESCRIPTION

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
62	64	80	82	X0	A (Oscillation)	Crystal oscillator pins
63	65	81	83	X1		
39 to 41	41 to 43	47 to 49	49 to 51	MD0 to MD2	F (CMOS)	Input pins for selecting operation modes Connect directly to V _{CC} or V _{SS} .
60	62	75	77	$\overline{\text{RST}}$	H (CMOS/H)	External reset request input
42	44	50	52	$\overline{\text{HST}}$	G (CMOS/H)	Hardware standby input pin
65 to 72	67 to 74	83 to 90	85 to 92	P00 to P07	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				AD00 to AD07		I/O pins for the lower 8-bit of the external address data bus This function is valid in the mode where the external bus is valid.
73 to 78, 79, 80	75 to 80, 1, 2	91 to 96, 97, 98	93 to 98, 99, 100	P10 to P15, P16, P17	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				AD08 to AD13, AD14, AD15		I/O pins for the upper 8-bit of the external address data bus This function is valid in the mode where the external bus is valid.
				WI0 to WI5, WI6, WI7		I/O pins for wake-up interrupts This function is valid in the single-chip mode. Because the input of the DTP/external interrupt circuit is used as required when the DTP/external interrupt circuit is enabled, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
1, 2, 3, 4	3, 4, 5, 6	99, 100, 1, 2	1, 2, 3, 4	P20, P21, P22, P23	B (CMOS)	General-purpose I/O port This function becomes valid in the single-chip mode or the external address output control register is set to select a port.
				A16, A17, A18, A19		Output pins for the external address bus of A16 to A19 This function is valid in the mode where the external bus is valid and the upper address control register is set to select an address.

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

(Continued)

MB90670/675 Series

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
5, 6	7, 8	3, 4	5, 6	P24, P25	E (CMOS/H)	General-purpose I/O port This function is always valid.
				TIN0, TIN1		Event input pins of 16-bit reload timer 0 and 1 Because this input is used as required when the 16-bit reload timer is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
7, 8	9, 10	5, 6	7, 8	P26, P27	E (CMOS/H)	General-purpose I/O port This function is valid when outputs from 16-bit reload timer 0 and 1 are disabled.
				TOT0, TOT1		Output pins for 16-bit reload timer 0 and 1 This function is valid when output from 16-bit reload timer 0 and 1 are enabled.
10	12	7	9	P30	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				ALE		Address latch enable output pin This function is valid in the mode where the external bus is valid.
11	13	8	10	P31	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode.
				RD		Read strobe output pin for the data bus This function is valid in the mode where the external bus is valid.
12	14	10	12	P32	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode or $\overline{\text{WRL}}/\overline{\text{WR}}$ pin output is disabled.
				$\overline{\text{WRL}}$		Write strobe output pin for the data bus This function is valid when $\overline{\text{WRL}}/\overline{\text{WR}}$ pin output is enabled in the mode where external bus is valid. $\overline{\text{WRL}}$ is used for holding the lower 8-bit for write strobe in 16-bit access operations, while $\overline{\text{WR}}$ is used for holding 8-bit data for write strobe in 8-bit access operations.
				$\overline{\text{WR}}$		
13	15	11	13	P33	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode, in the external bus 8-bit mode, or $\overline{\text{WRH}}$ pin output is disabled.
				$\overline{\text{WRH}}$		Write strobe output pin for the upper 8-bit of the data bus This function is valid when the external bus 16-bit mode is selected in the mode where the external bus is valid, and $\overline{\text{WRH}}$ output pin is enabled.

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

(Continued)

MB90670/675 Series

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
14	16	12	14	P34	B (CMOS)	General-purpose I/O port This function is valid when both the single-chip mode and the hold function are disabled.
				HRQ		Hold request input pin This function is valid in the mode where the external bus is valid or when the hold function is enabled.
15	17	13	15	P35	B (CMOS)	General-purpose I/O port This function is valid when both the single-chip mode and the hold function are disabled.
				$\overline{\text{HAK}}$		Hold acknowledge output pin This function is valid in the mode where the external bus is valid or when the hold function is enabled.
16	18	14	16	P36	B (CMOS)	General-purpose I/O port This function is valid when both the single-chip mode and the external ready function are disabled.
				RDY		Ready input pin This function is valid when the external ready function is enabled in the mode where the external bus is valid.
17	19	15	17	P37	B (CMOS)	General-purpose I/O port This function is valid in the single-chip mode or when the CLK output is disabled.
				CLK		CLK output pin This function is valid when CLK output is disabled in the mode where the external bus is valid.
18	20	16	18	P40	E (CMOS/H)	General-purpose I/O port This function is always valid.
				SIN0		Serial data input pin of UART0 Because this input is used as required when UART0 is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
19	21	17	19	P41	E (CMOS/H)	General-purpose I/O port This function is valid when serial data output from UART0 is disabled.
				SOT0		Serial data output pin of UART0 This function is valid when serial data output from UART0 is enabled.

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

(Continued)

MB90670/675 Series

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
20	22	18	20	P42	E (CMOS/H)	General-purpose I/O port This function is valid when clock output from UART0 is disabled.
				SCK0		Clock I/O pin of UART0 This function is valid when clock output from UART0 is enabled. Because this input is used as required when UART0 is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
21	23	19	21	P43	E (CMOS/H)	General-purpose I/O port This function is always valid.
				SIN1		Serial data input pin of UART1 (SCI) Because this input is used as required when UART1 (SCI) is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
22	24	20	22	P44	E (CMOS/H)	General-purpose I/O port This function is valid when serial data output from UART1 (SCI) is disabled.
				SOT1		Serial data output pin of UART1 (SCI) This function is valid when serial data output from UART1 (SCI) is enabled.
23	25	22	24	P45	E (CMOS/H)	General-purpose I/O port This function is valid when clock output from UART1 (SCI) is disabled.
				SCK1		Clock I/O pin of UART1 (SCI) This function is valid when clock output from UART1 (SCI) is enabled. Because this input is used as required when UART1 (SCI) is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
24	26	23	25	P46	E (CMOS/H)	General-purpose I/O port This function is valid when waveform output from 8/16-bit PPG timer 0 is disabled.
				PPG0		Output pin of 8/16-bit PPG timer 0 This function is valid when waveform output from 8/16-bit PPG timer 0 is enabled.

- *1: FPT-80P-M05
- *2: FPT-80P-M06
- *3: FPT-100P-M05
- *4: FPT-100P-M06

(Continued)

MB90670/675 Series

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
25	27	24	26	P47	E (CMOS/H)	General-purpose I/O port This function is always valid.
				$\overline{\text{ATG}}$		Trigger input pin of the 8/10-bit A/D converter Because this input is used as required when the 8/10-bit A/D converter is performing input operations, and it is necessary to stop outputs by other functions unless such outputs are made intentionally.
30, 31, 33, 34, 35 to 38	32, 33, 35, 36, 37 to 40	36, 37, 38, 39, 41 to 44	38, 39, 40, 41, 43 to 46	P50, P51, P52, P53, P54 to P57	C (CMOS/H)	I/O port of an open-drain type The input function is valid when the analog input enable register is set to select a port.
				AN0, AN1, AN2, AN3, AN4 to AN7		Analog input pins of the 8/10-bit A/D converter This function is valid when the analog input enable register is set to select AD.
43 to 46	45 to 48	51 to 54	53 to 56	P60 to P63	E (CMOS/H)	General-purpose I/O port This function is always valid.
				INT0 to INT3		Request input pins of the DTP/external interrupt circuit Because this input is used as required when the DTP/external interrupt circuit is performing input operations, and it is necessary to stop outputs from other functions unless such outputs are made intentionally.
47 to 50	49 to 52	55 to 58	57 to 60	P64 to P67	E (CMOS/H)	General-purpose I/O port This function is always valid.
				ASR0 to ASR3		Sample data input pins for ICU0 to ICU3 Because this input is used as required when the input capture (ICU) is performing input operations, and it is necessary to stop outputs from other functions unless such outputs are made intentionally.
51 to 58	53 to 60	59 to 66	61 to 68	P70 to P77	E (CMOS/H)	General-purpose I/O port This function is valid when waveform output from the output compare (OCU) is disabled.
				DOT0 to DOT7		Waveform output pins of OCU0 and OCU1 This function is valid when waveform output from the output compare (OCU) is enabled and output from the port is selected.

- *1: FPT-80P-M05
- *2: FPT-80P-M06
- *3: FPT-100P-M05
- *4: FPT-100P-M06

(Continued)

MB90670/675 Series

(Continued)

Pin no.				Pin name	Circuit type	Function
LQFP -80*1	QFP -80*2	LQFP -100*3	QFP -100*4			
59	61	25	27	P80	E (CMOS/H)	General-purpose I/O port This function is valid when waveform output from 8/16-bit PPG timer 1 is disabled.
				PPG1		Output pin of 8/16-bit PPG timer 1 This function is valid when waveform output from 8/16-bit PPG timer 1 is enabled.
—	—	26 to 31	28 to 33	P81 to P86	E (CMOS/H)	General-purpose I/O port This function is always valid.
—	—	45	47	P90	D (NMOS/H)	I/O port of an open-drain type This function is always valid.
				SDA		I/O pin of the I ² C interface This function is valid when operation of the I ² C interface is enabled. Hold the port output in the high-impedance status (PDR = 1) when the I ² C interface is in operation.
—	—	46	48	P91	D (NMOS/H)	I/O port of an open-drain type This function is always valid.
				SCL		Clock I/O pin of the I ² C interface This function is valid when operation of the I ² C interface is enabled. Hold the port output in the high-impedance status (PDR = 1) when the I ² C interface is in operation.
—	—	67 to 74	69 to 76	PA0 to PA7	E (CMOS/H)	General-purpose I/O port This function is always valid.
—	—	76 to 78	78 to 80	PB0 to PB2	E (CMOS/H)	General-purpose I/O port This function is always valid.
64	66	21, 82	23, 84	V _{cc}	Power supply	Power supply to the digital circuit
9, 32, 61	11, 34, 63	9, 40, 79	11, 42, 81	V _{ss}	Power supply	Ground level of the digital circuit
26	28	32	34	AV _{cc}	Power supply	Power supply to the analog circuit Make sure to turn on/turn off this power supply with a voltage exceeding AV _{cc} applied to V _{cc} .
27	29	33	35	AVRH	Power supply	Reference voltage input to the analog circuit Make sure to turn on/turn off this power supply with a voltage exceeding AVRH applied to AV _{cc} .
28	30	34	36	AVRL	Power supply	Reference voltage input to the analog circuit
29	31	35	37	AV _{ss}	Power supply	Ground level of the analog circuit

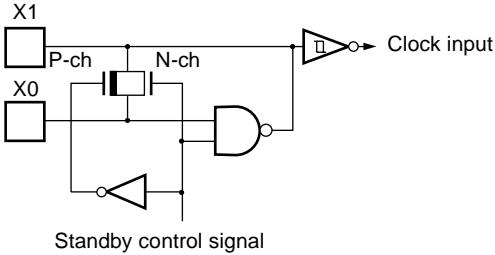
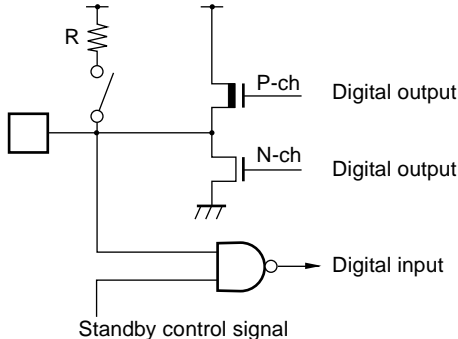
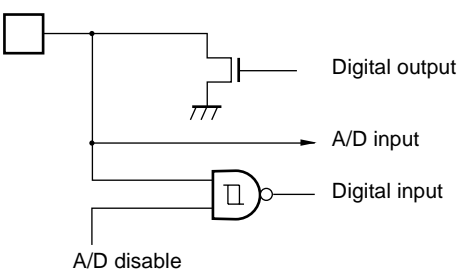
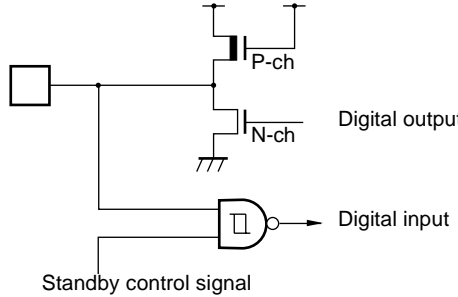
*1: FPT-80P-M05

*2: FPT-80P-M06

*3: FPT-100P-M05

*4: FPT-100P-M06

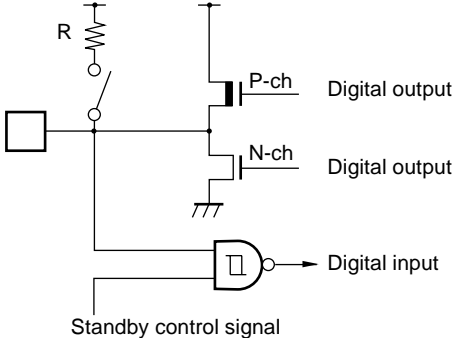
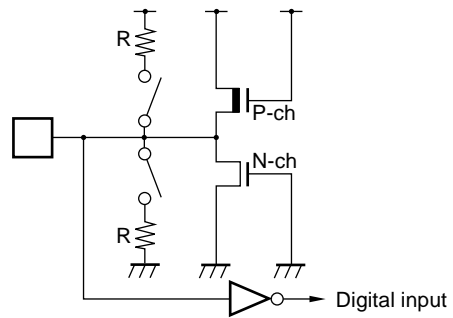
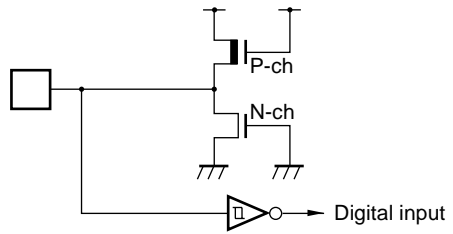
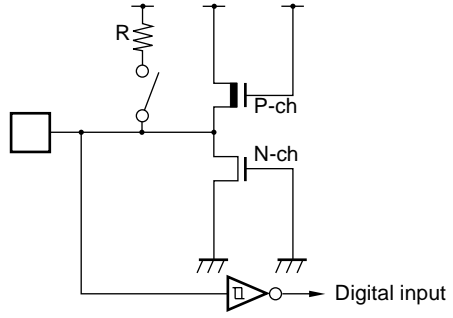
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> External clock frequency 3 MHz to 32 MHz Oscillation feedback resistor approx. 1MΩ
B		<ul style="list-style-type: none"> CMOS level input/output (with standby control) Pull-up option selectable (with standby control) No pull-up resistor in the MB90V670
C		<ul style="list-style-type: none"> N-ch open-drain output CMOS level hysteresis input (with A/D control)
D		<ul style="list-style-type: none"> NMOS open-drain output CMOS level hysteresis input (with standby control)

(Continued)

MB90670/675 Series

(Continued)

Type	Circuit	Remarks
E	 <p>The diagram shows a CMOS output stage. A pull-up resistor R is connected to the output node. A standby control signal is connected to the gates of both the P-channel and N-channel MOSFETs. The output node is connected to a digital input through an AND gate.</p>	<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input (with standby control) • Pull-up option selectable (with standby control) • No pull-up resistor in the MB90V670
F	 <p>The diagram shows a CMOS input stage. A pull-up resistor R is connected to the input node, and a pull-down resistor R is connected to ground. A standby control signal is connected to the gates of both the P-channel and N-channel MOSFETs. The input node is connected to a digital input through an inverter.</p>	<ul style="list-style-type: none"> • CMOS level input/output (without standby control) • Pull-up/pull-down option selectable (without stand-by control) • In mask ROM versions, MD2 pin is fixed to pull-down resistor, and optionally selectable the resistor in other pins. • The MB90V670 has no pull-up/pull-down resistors.
G	 <p>The diagram shows a CMOS input stage. A pull-up resistor R is connected to the input node. A standby control signal is connected to the gates of both the P-channel and N-channel MOSFETs. The input node is connected to a digital input through an inverter.</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input (without standby control)
H	 <p>The diagram shows a CMOS input stage. A pull-up resistor R is connected to the input node. A standby control signal is connected to the gates of both the P-channel and N-channel MOSFETs. The input node is connected to a digital input through an inverter.</p>	<ul style="list-style-type: none"> • CMOS level hysteresis input (without standby control) • Pull-up option selectable (without standby control) • No pull-up resistor in the MB90V670

■ HANDLING DEVICES

1. Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS} .

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC} , $AVRH$) and analog input voltages not exceed the digital voltage (V_{CC}).

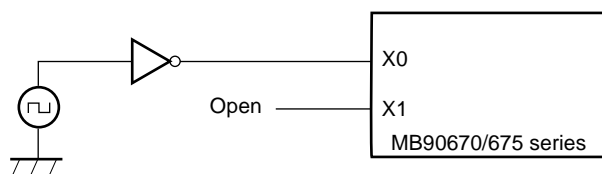
2. Connection of Unused Pins

Leaving unused pins open may result in abnormal operations. Clamp the pin level by connecting it to a pull-up or a pull-down resistor.

3. Notes on Using External Clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

• Using external clock



4. Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However, connect the pins external power and ground lines to lower the electro-magnetic emission level and abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around $0.1 \mu F$ between V_{CC} and V_{SS} pin near the device.

5. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with an grand area for stabilizing the operation.

6. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs ($AN0$ to $AN7$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

7. Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

8. “MOV @AL, AH”, “MOVW @AL, AH” Instructions

When the above instruction is performed to I/O space, an unnecessary writing operation ($\#FF$, $\#FFFF$) may be performed in the internal bus.

Use the compiler function for inserting an NOP instruction before the above instructions to avoid the writing operation.

Accessing RAM space with the above instruction does not cause any problem.

9. Initialization

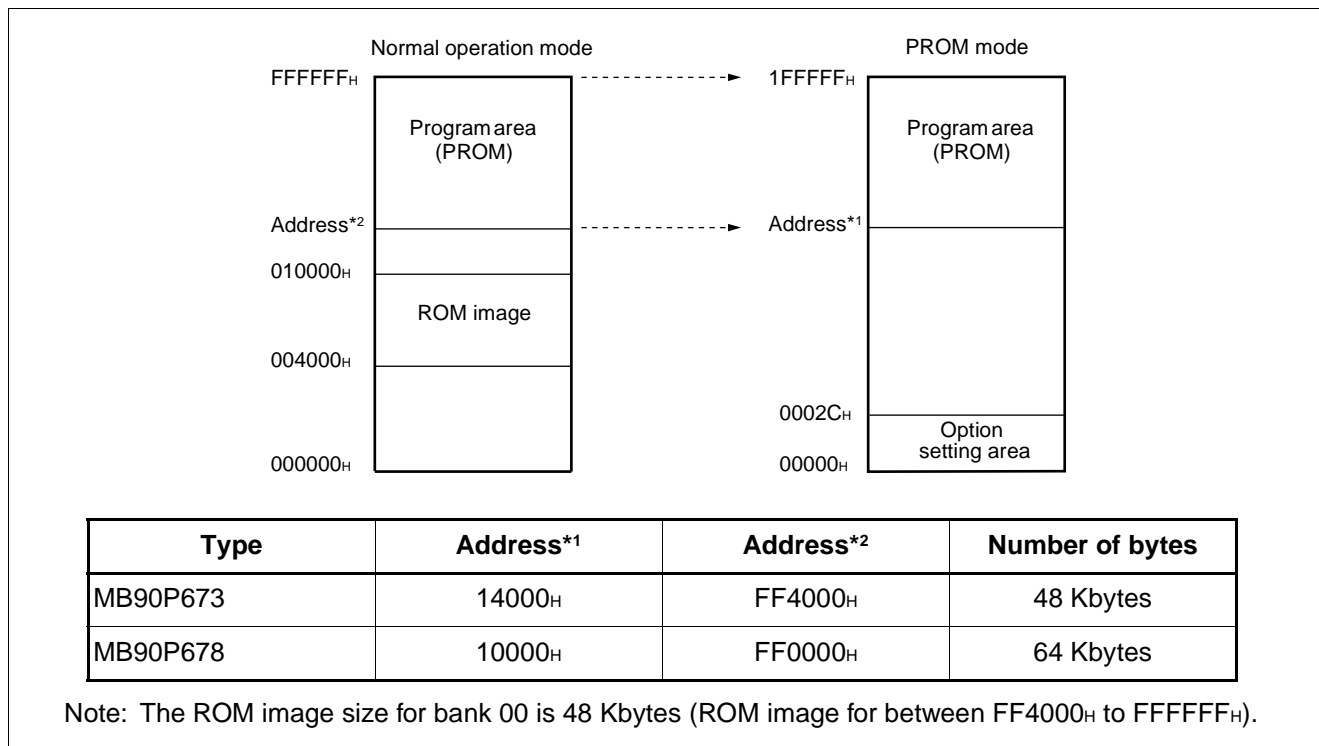
In the device, there are internal registers which is initialized only by a power-on reset. To initialize these registers, turning on the power again.

PROGRAMMING TO THE ONE-TIME PROM ON THE MB90P673/P678

The MB90P673 and MB90P678 has a PROM mode for emulation operation of the MBM27C1000/1000A, to which writing codes by a general-purpose ROM writer can be done via a dedicated adapter. Please note that the device is not compatible with the electronic signature (device ID code) mode.

1. Writing Sequence

The memory map for the PROM mode is shown as follows. Write option data to the option setting area according by referring to “7. PROM Option Bit Map”.



Write data to the one-time PROM microcontrollers according to the following sequence.

- (1) Set the PROM programmer to select the MBM27C1000/1000A.
- (2) Load the program data to the ROM programmer address *1 to 1FFFFH. To select a PROM option, load the option data from 00000H to 0002CH referring to “7. PROM Option Bit Map”.
- (3) Set the chip to the adapter socket and load the socket to the ROM programmer. Make sure that the device and adapter socket are properly oriented.
- (4) Program from 00000H to 1FFFFH.

Notes: • In mask-ROM products, there is no PROM mode and it is impossible to read data by a ROM programmer.
 • Contact sales personnel when purchasing a ROM programmer.

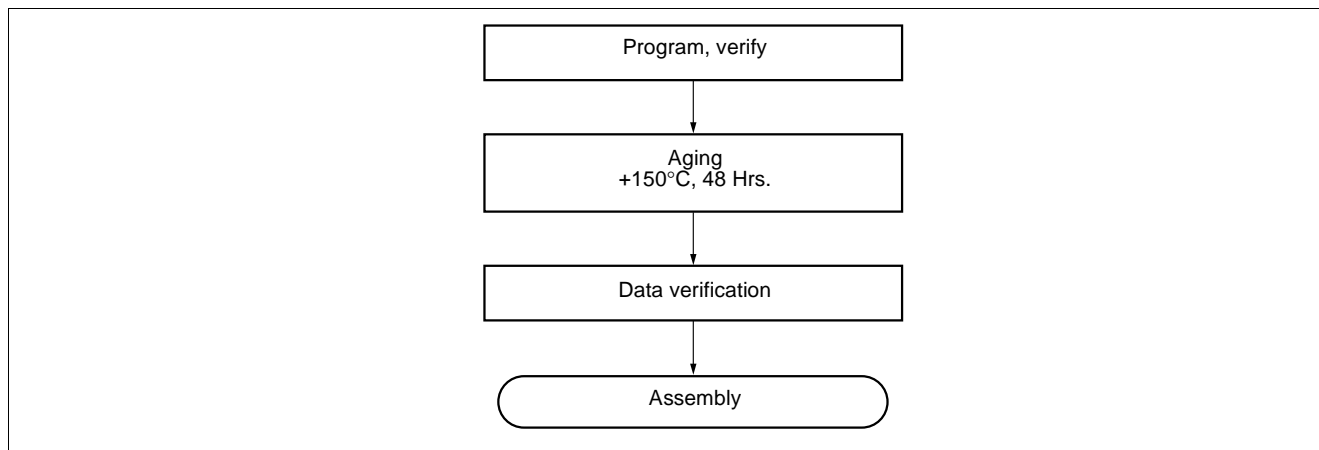
2. Program Mode

In the MB90P673/P678, all the bits are set to “1” upon shipping from FUJITSU or erasing operation. To write data, set desired bit selectively to “0”. However it is impossible to write electronically to the bits.

MB90670/675 Series

3. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked One-time PROM microcomputer program.



4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked One-time PROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

5. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part no.		MB90P673PF	MB90P673PFV	MB90P678PF	MB90P678PFV	
Package		QFP-80	LQFP-80	QFP-100	LQFP-100	
Compatible socket adapter Sun Hayato Co., Ltd.		ROM-80QF-32DP-16L	ROM-80SQF-32DP-16L	ROM-100QF-32DP-16L	ROM-100SQF-32DP-16L	
Recommended programmer manufacturer and programmer name	Minato Electronics Inc.	1890A	—	—	—	Recommended
		1891	—	—	—	Recommended
		1930	—	—	—	Recommended
	Data I/O Co., Ltd.	UNISITE	—	—	—	Recommended
		3900	—	—	—	Recommended
		2900	—	—	—	Recommended

Inquiry: San Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Minato Electronics Inc.: TEL: USA (1)-916-348-6066
JAPAN (81)-45-591-5611

Data I/O Co., Ltd.: TEL: USA/ASIA (1)-206-881-6444
EUROPE (49)-8-985-8580

MB90670/675 Series

6. Pin Assignment for EPROM Mode

- MBM27C1000/1000A pin compatible

MBM27C1000/1000A		MB90P673/MB90P678	
Pin no.	Pin name	Pin no.	Pin name
1	V _{PP}	Refer to pin assignments.	MD2
2	OE		P32
3	A15		P17
4	A12		P14
5	A07		P27
6	A06		P26
7	A05		P25
8	A04		P24
9	A03		P23
10	A02		P22
11	A01		P21
12	A00		P20
13	D00		P00
14	D01		P01
15	D02		P02
16	GND		V _{SS}

MBM27C1000/1000A		MB90P673/MB90P678	
Pin no.	Pin name	Pin no.	Pin name
32	V _{CC}	Refer to pin assignments.	V _{CC}
31	PGM		P33
30	N.C.		—
29	A14		P16
28	A13		P15
27	A08		P10
26	A09		P11
25	A11		P13
24	A16		P30
23	A10		P12
22	CE		P31
21	D07		P07
20	D06		P06
19	D05		P05
18	D04		P04
17	D03		P03

- Pin assignments for products not compatible with MBM27C1000/1000A

Pin no.	Pin name	processing
Refer to pin assignments.	MD0 MD1 X0	Connect a pull-up resistor of 4.7 k Ω .
	X1	OPEN
Refer to pin assignments.	AV _{CC} AVRH P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 P80 to P86 P90 P91 PA0 to PA7 PB0 to PB2	Connect a pull-up resistor having a resistance of approximately 1 M Ω to each pin.

- Power supply, GND connected pin

Type	Pin no.	Pin name
Power supply	Refer to pin assignments.	H \overline{ST} V _{CC}
		P34 P35 P36 R \overline{ST} AVRL AV _{SS} V _{SS}
GND	Refer to pin assignments.	

Note: Only MB90675 series has P81 to P86, P90, P91, PA0 to PA7, PB0 to PB2 pins.

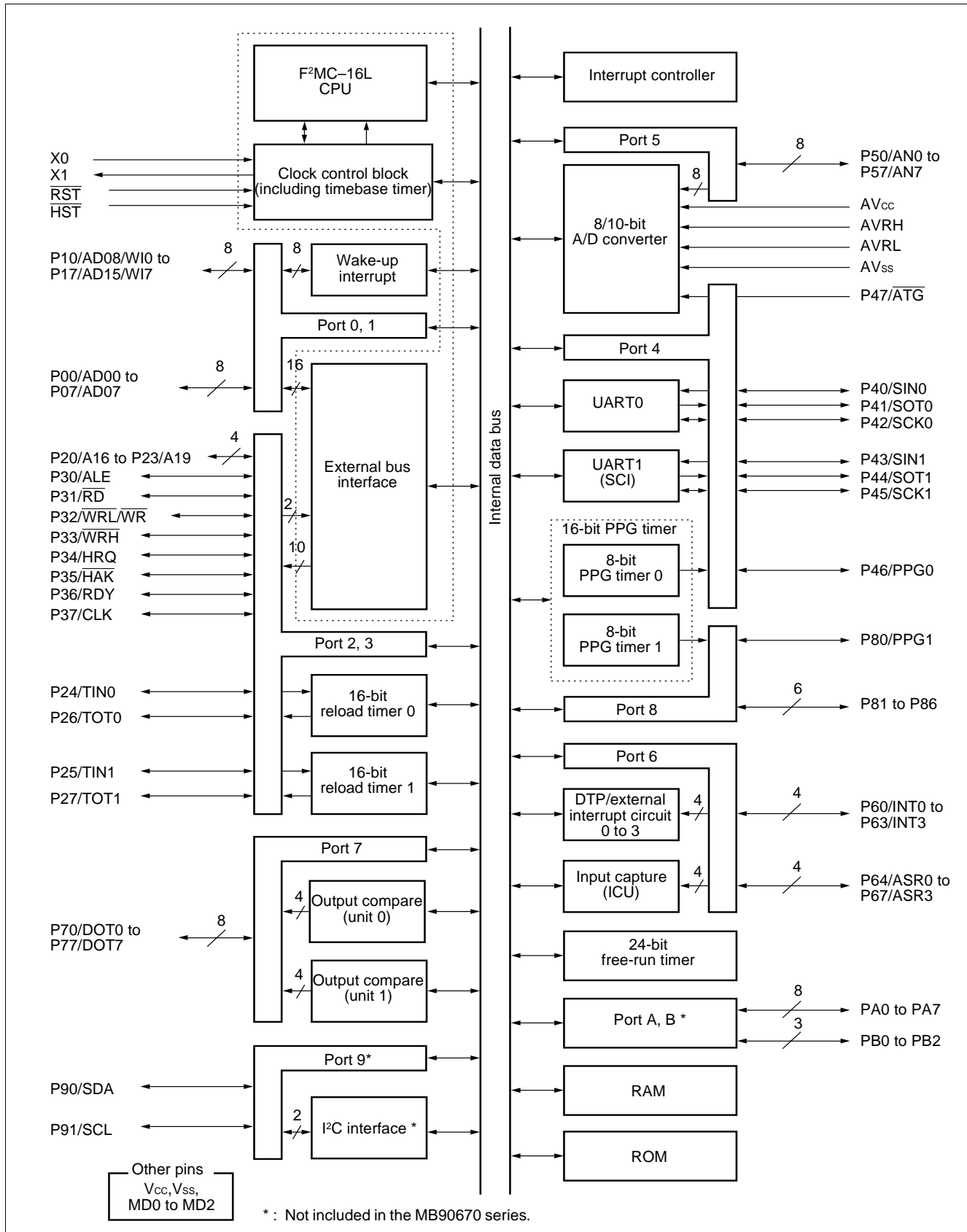
MB90670/675 Series

7. PROM Option Bit Map

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00000 _H	Vacancy	$\overline{\text{RST}}$ Pull-up 1: No 0: Yes	Vacancy	MD1 Pull-up 1: No 0: Yes	MD1 Pull-down 1: No 0: Yes	MD0 Pull-up 1: No 0: Yes	MD0 Pull-down 1: No 0: Yes	Vacancy
00004 _H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
00008 _H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0000C _H	P27 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
00010 _H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
00014 _H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0001C _H	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
00020 _H	P77 Pull-up 1: No 0: Yes	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
00024 _H	Vacancy	P86 Pull-up 1: No 0: Yes	P85 Pull-up 1: No 0: Yes	P84 Pull-up 1: No 0: Yes	P83 Pull-up 1: No 0: Yes	P82 Pull-up 1: No 0: Yes	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes
00028 _H	PA5 Pull-up 1: No 0: Yes	PA4 Pull-up 1: No 0: Yes	PA3 Pull-up 1: No 0: Yes	PA2 Pull-up 1: No 0: Yes	PA1 Pull-up 1: No 0: Yes	PA0 Pull-up 1: No 0: Yes	Vacancy	Vacancy
0002C _H	Vacancy	Vacancy	Vacancy	PB2 Pull-up 1: No 0: Yes	PB1 Pull-up 1: No 0: Yes	PB0 Pull-up 1: No 0: Yes	PA7 Pull-up 1: No 0: Yes	PA6 Pull-up 1: No 0: Yes

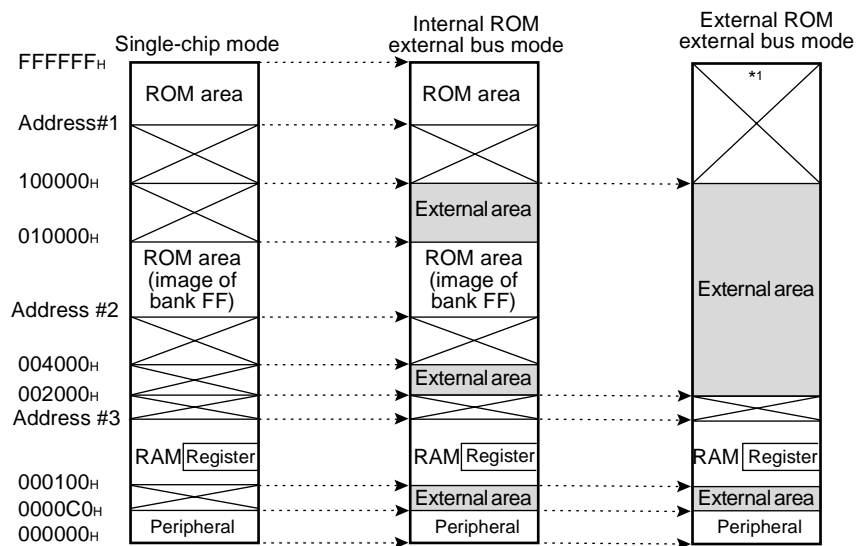
- Notes:
- Data "1" must be programmed to the reserved bits and address other than listed above.
 - Only MB90P678 has pull-up options for P81 to P86, PA0 to PA7, and PB0 to PB2 pins.
 - Data "1" must be programmed for the MB90P673.

■ BLOCK DIAGRAM






MB90670/675 Series

MEMORY MAP



Part number	Address #1*2	Address #2*2	Address #3*2
MB90671	FFC000H	00C000H	000380H
MB90672	FF8000H	008000H	000780H
MB90673	FF4000H	004000H	000900H
MB90T673	—	—	000900H
MB90P673	FF4000H	004000H	000900H
MB90676	FF8000H	008000H	000780H
MB90677	FF4000H	004000H	000900H
MB90678	FF0000H	004000H	000D00H
MB90T678	—	—	000D00H
MB90P678	FF0000H	004000H	000D00H

-  : Internal access memory
-  : External access memory
-  : Inhibited area

*1: The same external memory is accessed for bank 0F, 1F, 2F through FF.

*2: Addresses #1, #2 and #3 are unique to the product type.

Notes: • The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 is assigned to the same address, enabling reference of the table on the ROM without stating “far”.

However, the ROM area of the MB90678/P678 exceeds 48 Kbytes, and for this reason, the image from FF4000H to FFFFFFFH is reflected on bank 00 and image from FF0000H to FF3FFFH bank FF only.

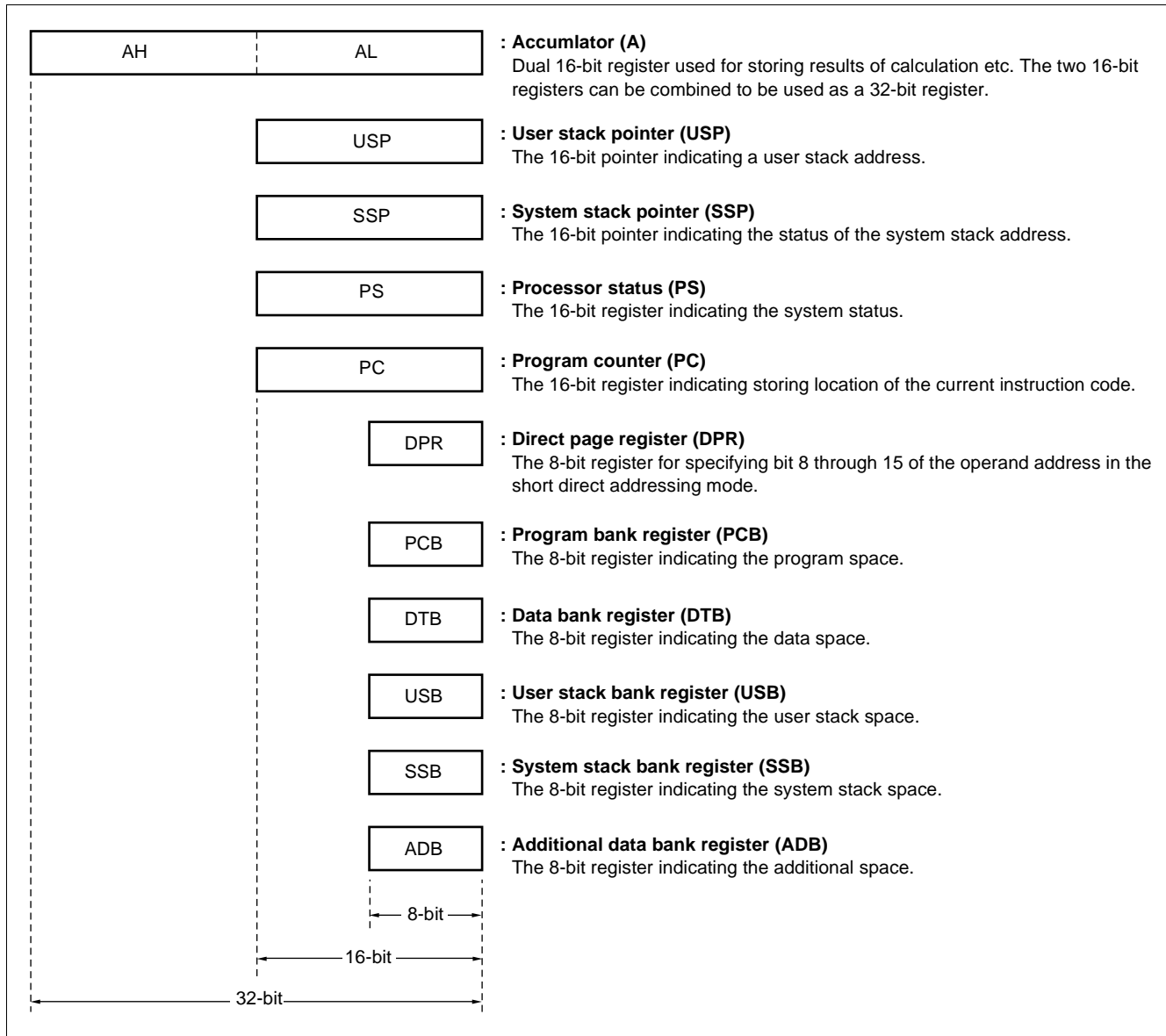
- In the MB90670/675 series, the upper 4-bit of the address are not output to the external bus. For this reason, the maximum area accessible is 1 Mbyte. The same address is accessed through different banks in different images.

For example, accessing “A00000H” and “B00000H” accesses the same address on the external bus.

- To prevent the memory or I/O from being accessed through images, and the data from being destroyed, it is recommended to limit number of banks to a maximum of 16 so that the banks are mapped without interfering each other. Caution must be also taken when masking the upper address with the external address output control register (HACR).

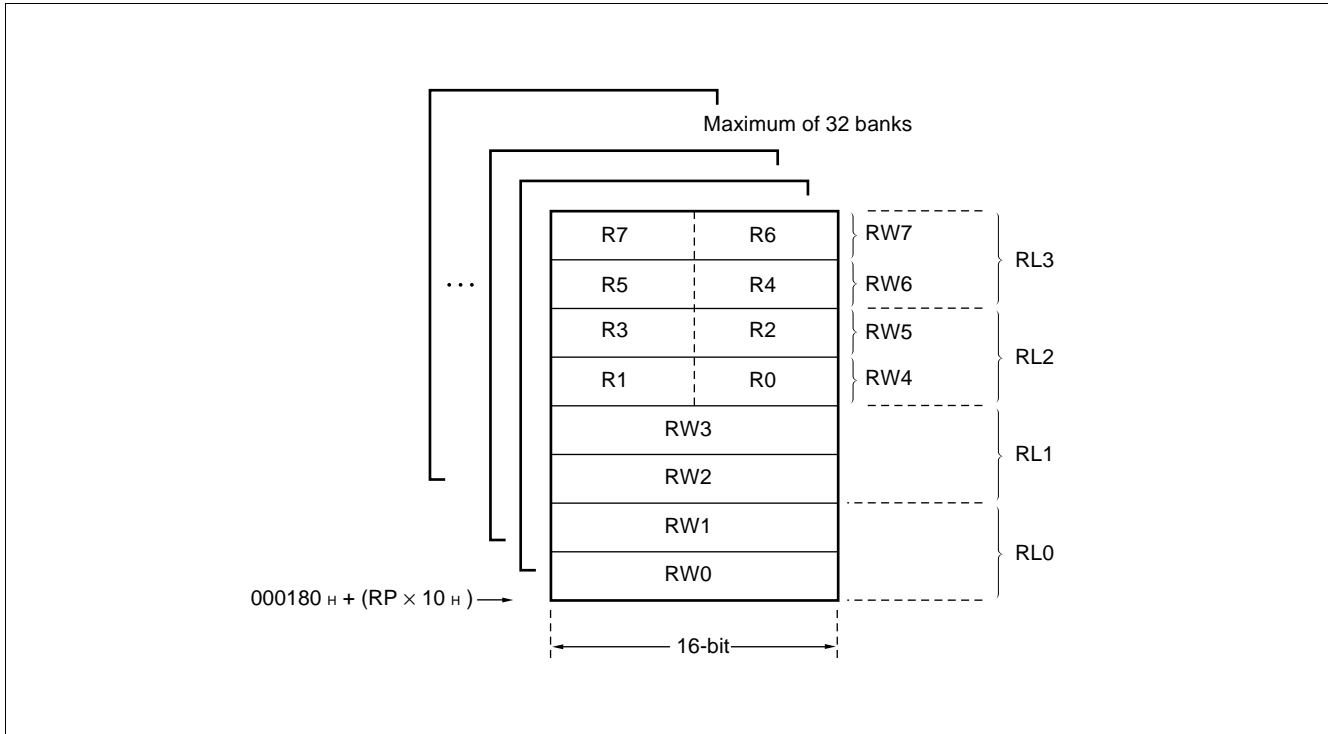
■ F²MC-16L CPU PROGRAMMING MODEL

(1) Dedicated Registers

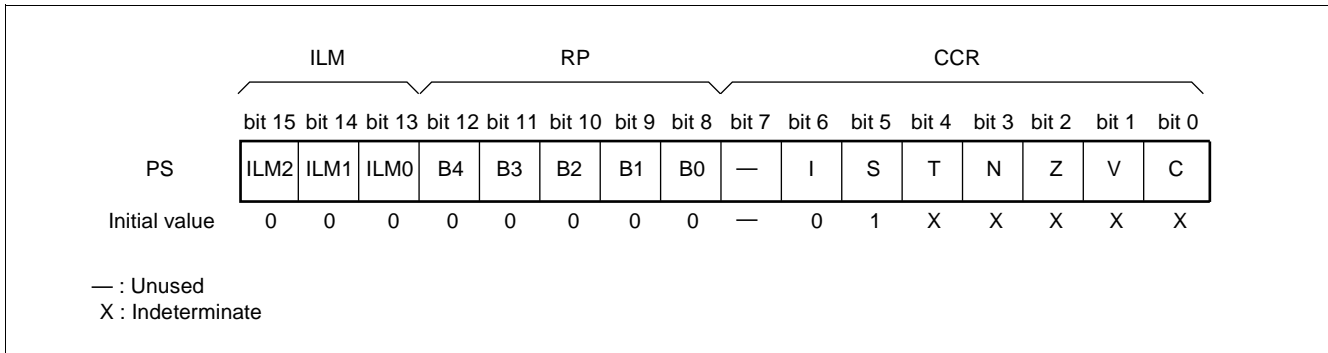


MB90670/675 Series

(2) General-purpose Registers



(3) Processor Status (PS)



MB90670/675 Series

■ I/O MAP

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000000 _H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXX _B
000001 _H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX _B
000002 _H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX _B
000003 _H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX _B
000004 _H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX _B
000005 _H	PDR5	Port 5 data register	R/W	Port 5	11111111 _B
000006 _H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXX _B
000007 _H	PDR7	Port 7 data register	R	Port 7	XXXXXXXX _B
000008 _H	PDR8	Port 8 data register	R/W	Port 8 ^{*5}	-XXXXXXXX _B
000009 _H	PDR9	Port 9 data register	R/W	Port 9 ^{*5}	-----11 _B
00000A _H	PDRA	Port A data register	R/W	Port A ^{*5}	XXXXXXXX _B
00000B _H	PDRB	Port B data register	R/W	Port B ^{*5}	-----XXX _B
00000C _H to 00000E _H	(Vacancy) ^{*3}				
00000F _H	EIFR	Wake-up interrupt flag register	R/W	Wake-up interrupt	-----0 _B
000010 _H	DDR0	Port 0 data direction register	R/W	Port 0	00000000 _B
000011 _H	DDR1	Port 1 data direction register	R/W	Port 1	00000000 _B
000012 _H	DDR2	Port 2 data direction register	R/W	Port 2	00000000 _B
000013 _H	DDR3	Port 3 data direction register	R/W	Port 3	00000000 _B
000014 _H	DDR4	Port 4 data direction register	R/W	Port 4	00000000 _B
000015 _H	ADER	Analog input enable register	R/W	Port 5, analog input	11111111 _B
000016 _H	DDR6	Port 6 data direction register	R/W	Port 6	00000000 _B
000017 _H	DDR7	Port 7 data direction register	R/W	Port 7	00000000 _B
000018 _H	DDR8	Port 8 data direction register	R/W	Port 8 ^{*5}	-0000000 _B
000019 _H	(Vacancy) ^{*3}				
00001A _H	DDRA	Port A data direction register	R/W	Port A ^{*5}	00000000 _B
00001B _H	DDRB	Port B data direction register	R/W	Port B ^{*5}	-----000 _B
00001C _H to 00001E _H	(Vacancy) ^{*3}				
00001F _H	EICR	Wake-up interrupt enable register	W	Wake-up interrupt	00000000 _B

(Continued)

MB90670/675 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000020H	UMC0	Mode control register 0	R/W!	UART0	0 0 0 0 0 1 0 0 _B
000021H	USR0	Status register 0	R/W!		0 0 0 1 0 0 0 0 _B
000022H	UIDR0/ UODR0	Input data register 0/ output data register 0	R/W		X X X X X X X X _B
000023H	URD0	Rate and data register 0	R/W		0 0 0 0 0 0 0 0 _B
000024H	SMR1	Mode register 1	R/W	UART1 (SCI)	0 0 0 0 0 0 0 0 _B
000025H	SCR1	Control register 1	R/W!		0 0 0 0 0 1 0 0 _B
000026H	SIDR1/ SODR1	Input data register 1/ output data register 1	R/W		X X X X X X X X _B
000027H	SSR1	Status register 1	R/W!		0 0 0 0 1 - 0 0 _B
000028H	ENIR	DTP/interrupt enable register	R/W	DTP/external interrupt circuit	- - - - 0 0 0 0 _B
000029H	EIRR	DTP/interrupt factor register	R/W		- - - - 0 0 0 0 _B
00002AH	ELVR	Request level setting register	R/W		0 0 0 0 0 0 0 0 _B
00002BH	(Vacancy) ^{*3}				
00002CH	ADCS	A/D convertor control status register	R/W!	8/10-bit A/D converter	0 0 0 0 0 0 0 0 _B
00002DH					0 0 0 0 0 0 0 0 _B
00002EH	ADCR	A/D convertor data register	R/W! ^{*4}		X X X X X X X X _B
00002FH					0 0 0 0 0 0 X X _B
000030H	PPGC0	PPG0 operating mode control register	R/W!	8/16-bit PPG timer 0	0 - 0 0 0 0 0 1 _B
000031H	PPGC1	PPG1 operating mode control register	R/W!	8/16-bit PPG timer 1	0 0 0 0 0 0 0 0 _B
000032H	(Vacancy) ^{*3}				
000033H	(Vacancy) ^{*3}				
000034H	PRL0	PPG0 reload register	R/W	8/16-bit PPG timer 0	X X X X X X X X _B
000035H	PRLH0		R/W		X X X X X X X X _B
000036H	PRL1	PPG1 reload register	R/W	8/16-bit PPG timer 1	X X X X X X X X _B
000037H	PRLH1		R/W		X X X X X X X X _B
000038H	TMCSR0	Timer control status register 0	R/W!	16-bit reload timer 0	0 0 0 0 0 0 0 0 _B
000039H					- - - - 0 0 0 0 _B
00003AH	TMR0/ TMRLR0	16-bit timer register 0/ 16-bit reload register 0	R/W		X X X X X X X X _B
00003BH					X X X X X X X X _B
00003CH	TMCSR1	Timer control status register 1	R/W!	16-bit reload timer 1	0 0 0 0 0 0 0 0 _B
00003DH					- - - - 0 0 0 0 _B
00003EH	TMR1/ TMRLR1	16-bit timer register 1/ 16-bit reload register 1	R/W		X X X X X X X X _B
00003FH					X X X X X X X X _B

(Continued)

MB90670/675 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
000040 _H	IBSR	I ² C bus status register	R	I ² C interface*6	0 0 0 0 0 0 0 0 _B
000041 _H	IBCR	I ² C bus control register	R/W		0 0 0 0 0 0 0 0 _B
000042 _H	ICCR	I ² C bus clock control register	R/W		-- 0 X X X X X _B
000043 _H	IADR	I ² C bus address register	R/W		- X X X X X X X _B
000044 _H	IDAR	I ² C bus data register	R/W		X X X X X X X X _B
000045 _H to 00004F _H	(Vacancy)*3				
000050 _H	TCCR	Free-run timer control register	R/W!	24-bit free-run timer	1 1 0 0 0 0 0 0 _B
000051 _H					-- 1 1 1 1 1 1 _B
000052 _H	ICC	ICU control register	R/W	Input capture (ICU)	0 0 0 0 0 0 0 0 _B
000053 _H					0 0 0 0 0 0 0 0 _B
000054 _H	TCRL	Free-run timer lower data register	R	24-bit free-run timer	0 0 0 0 0 0 0 0 _B
000055 _H					0 0 0 0 0 0 0 0 _B
000056 _H	TCRH	Free-run timer upper data register	R	24-bit free-run timer	0 0 0 0 0 0 0 0 _B
000057 _H					0 0 0 0 0 0 0 0 _B
000058 _H	CCR00	OCU control register 00	R/W	Output compare (OCU) (unit 0)	1 1 1 1 0 0 0 0 _B
000059 _H					---- 0 0 0 0 _B
00005A _H	CCR01	OCU control register 01	R/W	Output compare (OCU) (unit 0)	---- 0 0 0 0 _B
00005B _H					0 0 0 0 0 0 0 0 _B
00005C _H	CCR10	OCU control register 10	R/W	Output compare (OCU) (unit 1)	1 1 1 1 0 0 0 0 _B
00005D _H					---- 0 0 0 0 _B
00005E _H	CCR11	OCU control register 11	R/W	Output compare (OCU) (unit 1)	---- 0 0 0 0 _B
00005F _H					0 0 0 0 0 0 0 0 _B
000060 _H	ICDR0L	ICU lower data register 0	R	Input capture (ICU)	X X X X X X X X _B
000061 _H					X X X X X X X X _B
000062 _H	ICDR0H	ICU upper data register 0	R	Input capture (ICU)	X X X X X X X X _B
000063 _H					0 0 0 0 0 0 0 0 _B
000064 _H	ICDR1L	ICU lower data register 1	R	Input capture (ICU)	X X X X X X X X _B
000065 _H					X X X X X X X X _B
000066 _H	ICDR1H	ICU upper data register 1	R	Input capture (ICU)	X X X X X X X X _B
000067 _H					0 0 0 0 0 0 0 0 _B
000068 _H	ICDR2L	ICU lower data register 2	R	Input capture (ICU)	X X X X X X X X _B
000069 _H					X X X X X X X X _B

(Continued)

MB90670/675 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
00006AH	ICDR2H	ICU upper data register 2	R	Input capture (ICU)	XXXXXXXX _B
00006BH					00000000 _B
00006CH	ICDR3L	ICU lower data register 3	R		XXXXXXXX _B
00006DH					XXXXXXXX _B
00006EH	ICDR3H	ICU upper data register 3	R		XXXXXXXX _B
00006FH					00000000 _B
000070H	CPR00L	OCU compare lower data register 0	R/W	Output compare (OCU) (unit 0)	00000000 _B
000071H					00000000 _B
000072H	CPR00H	OCU compare upper data register 0	R/W		00000000 _B
000073H					00000000 _B
000074H	CPR01L	OCU compare lower data register 1	R/W		00000000 _B
000075H					00000000 _B
000076H	CPR01H	OCU compare upper data register 1	R/W		00000000 _B
000077H					00000000 _B
000078H	CPR02L	OCU compare lower data register 2	R/W		00000000 _B
000079H					00000000 _B
00007AH	CPR02H	OCU compare upper data register 2	R/W		00000000 _B
00007BH					00000000 _B
00007CH	CPR03L	OCU compare lower data register 3	R/W		00000000 _B
00007DH					00000000 _B
00007EH	CPR03H	OCU compare upper data register 3	R/W		00000000 _B
00007FH					00000000 _B
000080H	CPR04L	OCU compare lower data register 4	R/W		00000000 _B
000081H					00000000 _B
000082H	CPR04H	OCU compare upper data register 4	R/W		00000000 _B
000083H					00000000 _B
000084H	CPR05L	OCU compare lower data register 5	R/W		00000000 _B
000085H					00000000 _B
000086H	CPR05H	OCU compare upper data register 5	R/W		00000000 _B
000087H					00000000 _B
000088H	CPR06L	OCU compare lower data register 6	R/W	00000000 _B	
000089H				00000000 _B	
00008AH	CPR06H	OCU compare upper data register 6	R/W	00000000 _B	
00008BH				00000000 _B	

(Continued)

MB90670/675 Series

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
00008C _H	CPR07L	OCU compare lower data register 7	R/W	Output compare (OCU) (unit 1)	0 0 0 0 0 0 0 0 _B
00008D _H					0 0 0 0 0 0 0 0 _B
00008E _H	CPR07H	OCU compare upper data register 7	R/W		0 0 0 0 0 0 0 0 _B
00008F _H					0 0 0 0 0 0 0 0 _B
000090 _H to 00009E _H	(System reservation area)* ¹				
00009F _H	DIRR	Delayed interrupt factor generation/cancellation register	R/W	Delayed interrupt generation module	----- 0 _B
0000A0 _H	LPMCR	Low-power consumption mode control register	R/W!	Low-power consumption (stand-by) mode	0 0 0 1 1 0 0 0 _B
0000A1 _H	CKSCR	Clock selection register	R/W!	Low-power consumption (stand-by) mode	1 1 1 1 1 1 0 0 _B
0000A2 _H to 0000A4 _H	(Vacancy)* ³				
0000A5 _H	ARSR	Automatic ready function select register	W	External bus pin	0 0 1 1 -- 0 0 _B
0000A6 _H	HACR	Upper address control register	W	External bus pin	---- 0 0 0 0 _B
0000A7 _H	EPCR	Bus control signal select register	W	External bus pin	0 0 0 0 * 0 0 - _B
0000A8 _H	WDTC	Watchdog timer control register	R/W!	Watchdog timer	X X X X X 1 1 1 _B
0000A9 _H	TBTC	Timebase timer control register	R/W!	Timebase timer	1 -- 0 0 1 0 0 _B
0000AA _H to 0000AF _H	(Vacancy)* ³				
0000B0 _H	ICR00	Interrupt control register 00	R/W!	Interrupt controller	0 0 0 0 0 1 1 1 _B
0000B1 _H	ICR01	Interrupt control register 01	R/W!		0 0 0 0 0 1 1 1 _B
0000B2 _H	ICR02	Interrupt control register 02	R/W!		0 0 0 0 0 1 1 1 _B
0000B3 _H	ICR03	Interrupt control register 03	R/W!		0 0 0 0 0 1 1 1 _B
0000B4 _H	ICR04	Interrupt control register 04	R/W!		0 0 0 0 0 1 1 1 _B
0000B5 _H	ICR05	Interrupt control register 05	R/W!		0 0 0 0 0 1 1 1 _B
0000B6 _H	ICR06	Interrupt control register 06	R/W!		0 0 0 0 0 1 1 1 _B
0000B7 _H	ICR07	Interrupt control register 07	R/W!		0 0 0 0 0 1 1 1 _B
0000B8 _H	ICR08	Interrupt control register 08	R/W!		0 0 0 0 0 1 1 1 _B
0000B9 _H	ICR09	Interrupt control register 09	R/W!		0 0 0 0 0 1 1 1 _B

(Continued)

MB90670/675 Series

(Continued)

Address	Abbreviated register name	Register name	Read/write	Resource name	Initial value
0000BA _H	ICR10	Interrupt control register 10	R/W!	Interrupt controller	0 0 0 0 0 1 1 1 _B
0000BB _H	ICR11	Interrupt control register 11	R/W!		0 0 0 0 0 1 1 1 _B
0000BC _H	ICR12	Interrupt control register 12	R/W!		0 0 0 0 0 1 1 1 _B
0000BD _H	ICR13	Interrupt control register 13	R/W!		0 0 0 0 0 1 1 1 _B
0000BE _H	ICR14	Interrupt control register 14	R/W!		0 0 0 0 0 1 1 1 _B
0000BF _H	ICR15	Interrupt control register 15	R/W!		0 0 0 0 0 1 1 1 _B
0000C0 _H to 0000FF _H	(External area)*2				

Descriptions for read/write

R/W: Readable and writable

R: Read only

W: Write only

R/W!: Bits for reading operation only or writing operation only are included. Refer to the register lists for specific resource for detailed information.

Descriptions for initial value

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

* : The initial value of this bit is "1" or "0" (decided by levels on pins of MD0 through MD2).

X : The initial value of this bit is indeterminate.

– : This bit is not used. The initial value is indeterminate.

*1: Access prohibited.

*2: This area is the only external access area having an address of 0000FF_H or lower. An access operation to this area is handled as that to external I/O area.

*3: The area corresponding to the "(Vacancy)" on the I/O map is reserved, and accessing operation to this area is handled as that to internal area. No access signal to external devices are generated.

*4: Only bit 15 is writable. Reading bit 10 through bit 15 returns "0" as a reading result.

*5: In the MB90670 series, P81 through P86, P90, P91, PA0 through PA7, PB0 through PB2 are not present. For this reason, bits corresponding to these pins are not used.

*6: The MB90670 series does not have the I²C interface. For this reason, this area is "(Vacancy)" in the MB90670 series.

Note: For bits that is only allowed to program, the initial value set by the reset operation is listed as an initial value. Note that the values are different from reading results.

For LPMCR/CKSCR/WDTC, there are cases where initialization is performed or not performed, depending on the types of the reset. However initial value for resets that initializes the value are listed.

MB90670/675 Series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt source	E ² OS support	Interrupt vector		Interrupt control register		Priority*4	
		Number	Address	ICR	Address		
Reset	×	# 08	08 _H	FFFFDC _H	—	High ↑	
INT9 instruction	×	# 09	09 _H	FFFFD8 _H	—		
Exception	×	# 10	0A _H	FFFFD4 _H	—		
DTP/external interrupt circuit Channel 0	△	# 11	0B _H	FFFFD0 _H	ICR00		0000B0 _H *2
DTP/external interrupt circuit Channel 1	△	# 12	0C _H	FFFFCC _H			
DTP/external interrupt circuit Channel 2	△	# 13	0D _H	FFFFC8 _H	ICR01		0000B1 _H *2
DTP/external interrupt circuit Channel 3	△	# 14	0E _H	FFFFC4 _H			
Output compare Channel 0	△	# 15	0F _H	FFFFC0 _H	ICR02		0000B2 _H *2
Output compare Channel 1	△	# 16	10 _H	FFFFBC _H			
Output compare Channel 2	△	# 17	11 _H	FFFFB8 _H	ICR03		0000B3 _H *2
Output compare Channel 3	△	# 18	12 _H	FFFFB4 _H			
Output compare Channel 4	△	# 19	13 _H	FFFFB0 _H	ICR04	0000B4 _H *2	
Output compare Channel 5	△	# 20	14 _H	FFFFAC _H			
Output compare Channel 6	△	# 21	15 _H	FFFFA8 _H	ICR05	0000B5 _H *2	
Output compare Channel 7	△	# 22	16 _H	FFFFA4 _H			
24-bit free-run timer Overflow	△	# 23	17 _H	FFFFA0 _H	ICR06	0000B6 _H *2	
24-bit free-run timer Intermediate bit	△	# 24	18 _H	FFFF9C _H			
Input capture Channel 0	△	# 25	19 _H	FFFF98 _H	ICR07	0000B7 _H *2	
Input capture Channel 1	△	# 26	1A _H	FFFF94 _H			
Input capture Channel 2	△	# 27	1B _H	FFFF90 _H	ICR08	0000B8 _H *2	
Input capture Channel 3	△	# 28	1C _H	FFFF8C _H			
16-bit reload timer/ 8/16-bit PPG timer 0	△	# 29	1D _H	FFFF88 _H	ICR09	0000B9 _H *2, *3	
16-bit reload timer/ 8/16-bit PPG timer 1	△	# 30	1E _H	FFFF84 _H			
8/10-bit A/D converter measurement complete	○	# 31	1F _H	FFFF80 _H	ICR10	0000BA _H	
Wake-up interrupt	×	# 33	21 _H	FFFF78 _H	ICR11	0000BB _H *2	
Timebase timer interval interrupt	×	# 34	22 _H	FFFF74 _H			

(Continued)

(Continued)

Interrupt source	EI ² OS support	Interrupt vector			Interrupt control register		Priority* ⁴
		Number	Address	ICR	Address		
UART1 (SCI) transmission complete	△	# 35	23 _H	FFFF70 _H	ICR12	0000BC _H * ²	↑ High ↓ Low
UART0 transmission complete	△	# 36	24 _H	FFFF6C _H			
UART1 (SCI) reception complete	◎	# 37	25 _H	FFFF68 _H	ICR13	0000BD _H * ²	
I ² C interface* ¹	×	# 38	26 _H	FFFF64 _H			
UART0 reception complete	◎	# 39	27 _H	FFFF60 _H	ICR14	0000BE _H	
Delayed interrupt generation module	×	# 42	2A _H	FFFF54 _H	ICR15	0000BF _H	

○ : Can be used

× : Can not be used

◎ : Can be used. With EI²OS stop function.

△ : Can be used if interrupt request using ICR are not commonly used.

*1: In MB90670 series, this interrupt vector is not used because the series does not have the I²C interface.

*2: • Interrupt levels for peripherals that commonly use the ICR register are in the same level.

• When the extended intelligent I/O service (EI²OS) is specified in a peripheral device commonly using the ICR register, only one of the functions can be used.

• When the extended intelligent I/O service (EI²OS) is specified for one of the peripheral functions, interrupts can not be used on the other function.

*3: Only 16-bit reload timer conforms to the extended intelligent I/O service (EI²OS). Because the 8/16-bit PPG timer does not conform to the extended intelligent I/O service (EI²OS), disable interrupts of the 8/16-bit PPG timer when using the extended intelligent I/O service (EI²OS) in the 16-bit reload timer.

*4: The level shows priority of same level of interrupt invoked simultaneously.

MB90670/675 Series

■ PERIPHERALS

1. I/O Port

(1) Input/output Port

Port 0 to 4, 6, 8, A, and B are general-purpose I/O ports having a combined function as an external bus pin and a resource input. The input output ports function as general-purpose I/O port only in the single-chip mode. In the external bus mode, the ports are configured as external bus pins, and part of pins for port 3 can be configured as general-purpose I/O port by setting the bus control signal select register (ECSR). Each pin corresponding to upper 4-bit of the port 2 can be switched between a resource and a port bitwise.

Only MB90675 series has port A and port B.

- Operation as output port

The pin is configured as an output port by setting the corresponding bit of the DDR register to "1".

Writing data to PDR register when the port is configured as output, the data is retained in the output latch in the PDR and directly output to the pin.

The value of the pin (the same value retained in the output latch of PDR) can be read out by reading the PDR register.

Note: When a read-modify-write instruction (e.g. bit set instruction) is performed to the port data register, the destination bit of the operation is set to the specified value, not affecting the bits configured by the DDR register for output, however, values of bits configured by the DDR register as inputs are changed because input values to the pins are written into the output latch. To avoid this situation, configure the pins by the DDR register as output after writing output data to the PDR register when configuring the bit used as input as outputs.

- Operation as input port

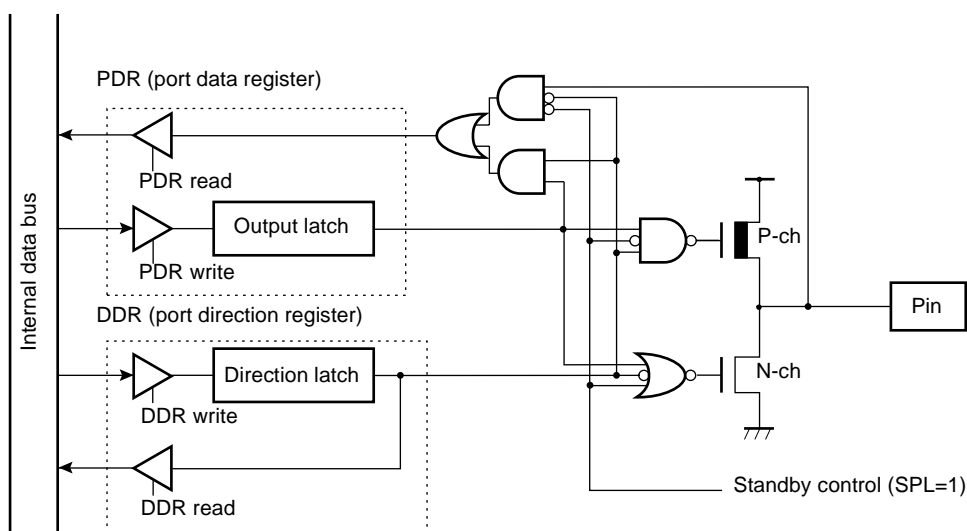
The pin is configured as an input by setting the corresponding bit of the DDR register to "0".

When the pin is configured as an input, the output buffer is turned-off and the pin is put into a high-impedance status.

When a data is written into the PDR register, the data is retained in the output latch of the PDR, but pin outputs are unaffected.

Reading the PDR register reads out the pin level ("0" or "1").

- Block diagram



Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

(2) N-ch Open-drain Port

Port 5 and port 9 are general-purpose I/O ports having a combined function as resource input/output. Each pin can be switched between resource and port bitwise.

Only MB90675 series has port 9.

- Operation as output port

When a data is written into the PDR register, the data is latched to the output latch of PDR. When the output latch value is set to "0", the output transistor is turned on and the pin status is put into an "L" level output, while writing "1" turns off the transistor and put the pin in a high-impedance status.

If the output pin is pulled-up, setting output latch value to "1" puts the pin in the pull-up status.

Reading the PDR register returns the pin value (same as the output latch value in the PDR).

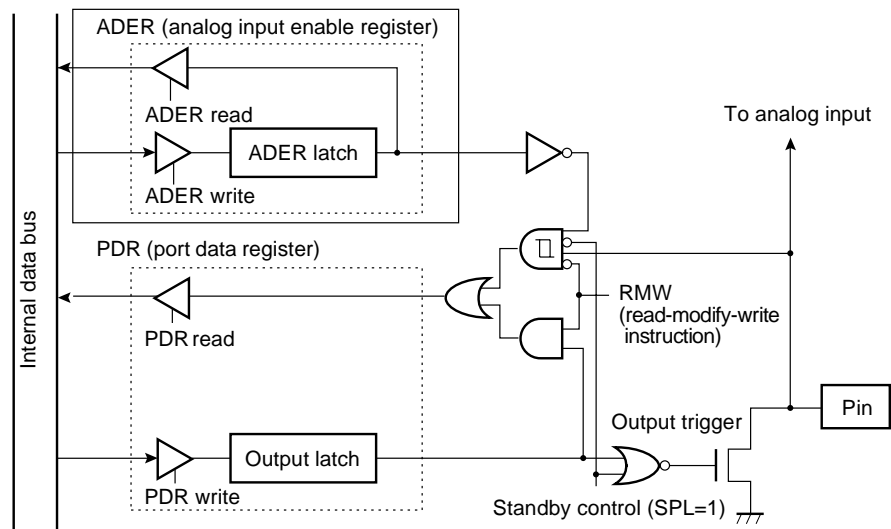
Note: Execution of a read-modify-write instruction (e.g. bit set instruction) reads out the output latch value rather than the pin value, leaving output latch that is not manipulated unchanged.

- Operation as input port

Setting corresponding bit of the PDR register to "1" turns off the output transistor and the pin is put into a high-impedance status.

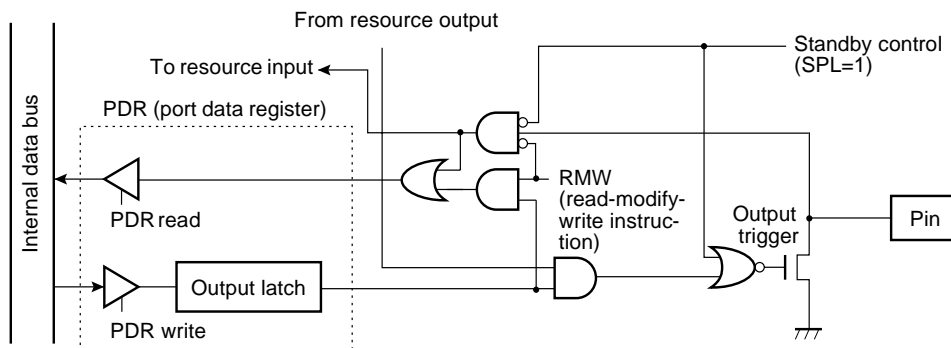
Reading the PDR register returns the pin level ("0" or "1").

- Block diagram of port 5



Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

- Block diagram of port 9



Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

MB90670/675 Series

(3) Output Port

Port 7 is a general-purpose output port having a combined function as an output compare (OCU) output. Note that only OCU output can be output when the pin is configured as an output, and it is not used for outputting given data by writing to the data register. Each pin can be switched between an output compare output and a port bitwise.

- Operation as output port (operation of OCU output)

Setting the corresponding bit of the DDR register to “1” configures the pin as an output port. In this case, lower 4-bit of CCR01 and CCR register are output.

When configured as an output, the output buffer is turned on and data retained in the output latch in the PDR of the output compare is output to the pin.

Writing data to DOT bit of the OCU control register (CCR01, CCR11) corresponding to each pin writes data in synchronization to a match operation of the output compare and output to the pin.

Reading the PDR register returns the pin level (same as the output latch value of the PDR).

When output of output compare is enabled, an output value from the output compare can be read out.

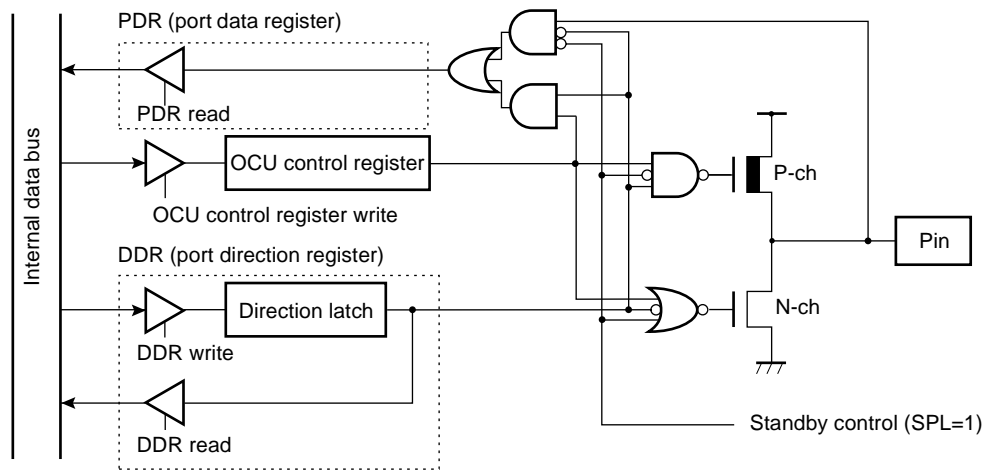
- Operation as input port

Setting corresponding bit of the DDR register to “0” configures the pin as input port.

When the pin is configured as an input port, the output buffer is turned off and the pin is put into a high-impedance status.

Reading the PDR register returns the pin level (“0” or “1”).

- Block diagram



Standby control: Stop, timebase timer mode and SPL=1, or hardware standby mode

(4) Register Configuration

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000000H	(PDR1)								P07	P06	P05	P04	P03	P02	P01	P00	Port 0 data register (PDR0)
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000001H	P17	P16	P15	P14	P13	P12	P11	P10	(PDR0)								Port 1 data register (PDR1)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000002H	(PDR3)								P27	P26	P25	P24	P23	P22	P21	P20	Port 2 data register (PDR2)
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000003H	P37	P36	P35	P34	P33	P32	P31	P30	(PDR2)								Port 3 data register (PDR3)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000004H	(PDR5)								P47	P46	P45	P44	P43	P42	P41	P40	Port 4 data register (PDR4)
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000005H	P57	P56	P55	P54	P53	P52	P51	P50	(PDR4)								Port 5 data register (PDR5)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000006H	(PDR7)								P67	P66	P65	P64	P63	P62	P61	P60	Port 6 data register (PDR6)
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000007H	P77	P76	P75	P74	P73	P72	P71	P70	(PDR6)								Port 7 data register (PDR7)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000008H	(PDR9)								—	P86	P85	P84	P83	P82	P81	P80	Port 8 data register (PDR8)
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000009H	—	—	—	—	—	—	P91	P90	(PDR8)								Port 9 data register (PDR9)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
00000AH	(PDRB)								PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A data register (PDRA)
									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
00000BH	—	—	—	—	—	PB2	PB1	PB0	(PDRA)								Port B data register (PDRB)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W								

(Continued)

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(Continued)

Address	bit-15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000010 _H	(DDR1)			P07	P06	P05	P04	P03	P02	P01	P00	Port 0 data direction register (DDR0)
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	
000011 _H	P17	P16	P15	P14	P13	P12	P11	P10	(DDR0)			Port 1 data direction register (DDR1)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000012 _H	(DDR3)			P27	P26	P25	P24	P23	P22	P21	P20	Port 2 data direction register (DDR2)
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	
000013 _H	P37	P36	P35	P34	P33	P32	P31	P30	(DDR2)			Port 3 data direction register (DDR3)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000014 _H	(ADER)			P47	P46	P45	P44	P43	P42	P41	P40	Port 4 data direction register (DDR4)
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	
000015 _H	P57	P56	P55	P54	P53	P52	P51	P50	(DDR4)			Analog input enable register (ADER)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000016 _H	(DDR7)			P67	P66	P65	P64	P63	P62	P61	P60	Port 6 data direction register (DDR6)
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	
000017 _H	P77	P76	P75	P74	P73	P72	P71	P70	(DDR6)			Port 7 data direction register (DDR7)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
000018 _H	(Vacancy)			—	P86	P85	P84	P83	P82	P81	P80	Port 8 data direction register (DDR8)
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
00001A _H	(DDRB)			PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A data direction register (DDRA)
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	
00001B _H	—	—	—	—	—	PB2	PB1	PB0	(DDRA)			Port B data direction register (DDR8)
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

Note: Only MB90675 series has P81 through P86, P90, PA0 through PA7, and PB0 through PB2, and MB90670 series does not have such pins.

2. Timebase Timer

The timebase timer is a 18-bit free-run counter (timebase counter) for counting up in synchronization to the internal count clock (divided-by-2 of oscillation) with an interval timer function for selecting an interval time from four types of $2^{12}/\text{HCLK}$, $2^{14}/\text{HCLK}$, $2^{16}/\text{HCLK}$, and $2^{19}/\text{HCLK}$.

The timebase timer also has a function for supplying operating clocks for the timer output for the oscillation stabilization time or the watchdog timer etc.

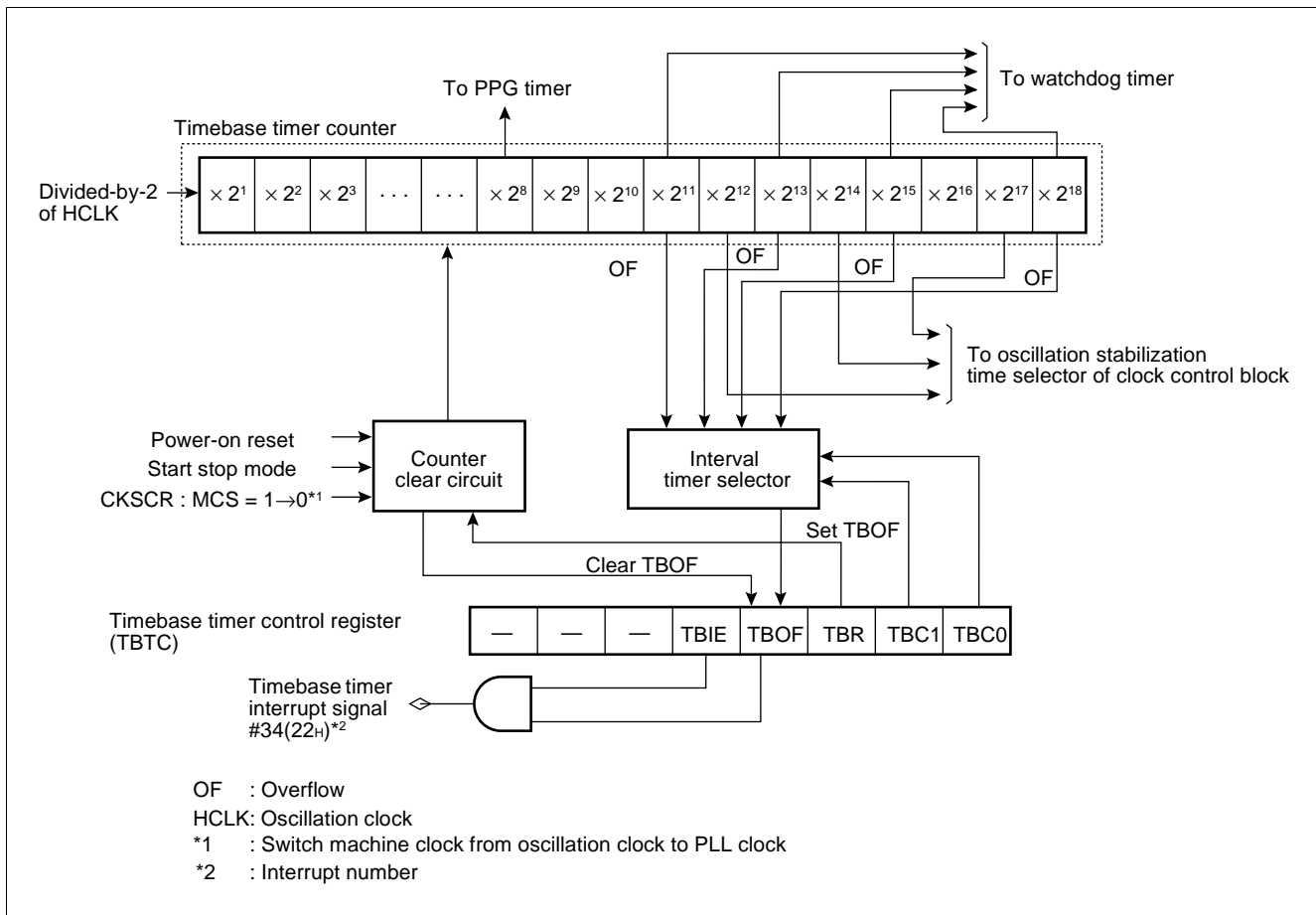
(1) Register Configuration

- Timebase timer control register (TBTC)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
0000A9 _H	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0	(WDTC)			1--00100 _B
	R/W	—	—	R/W	R/W	W	R/W	R/W				

R/W: Readable and writable
 W : Read only
 — : Unused

(2) Block Diagram



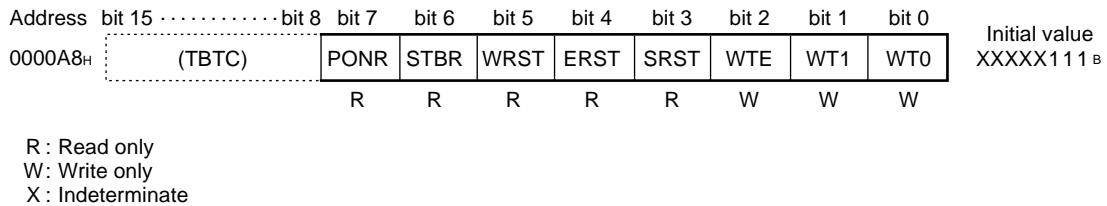
MB90670/675 Series

3. Watchdog Timer

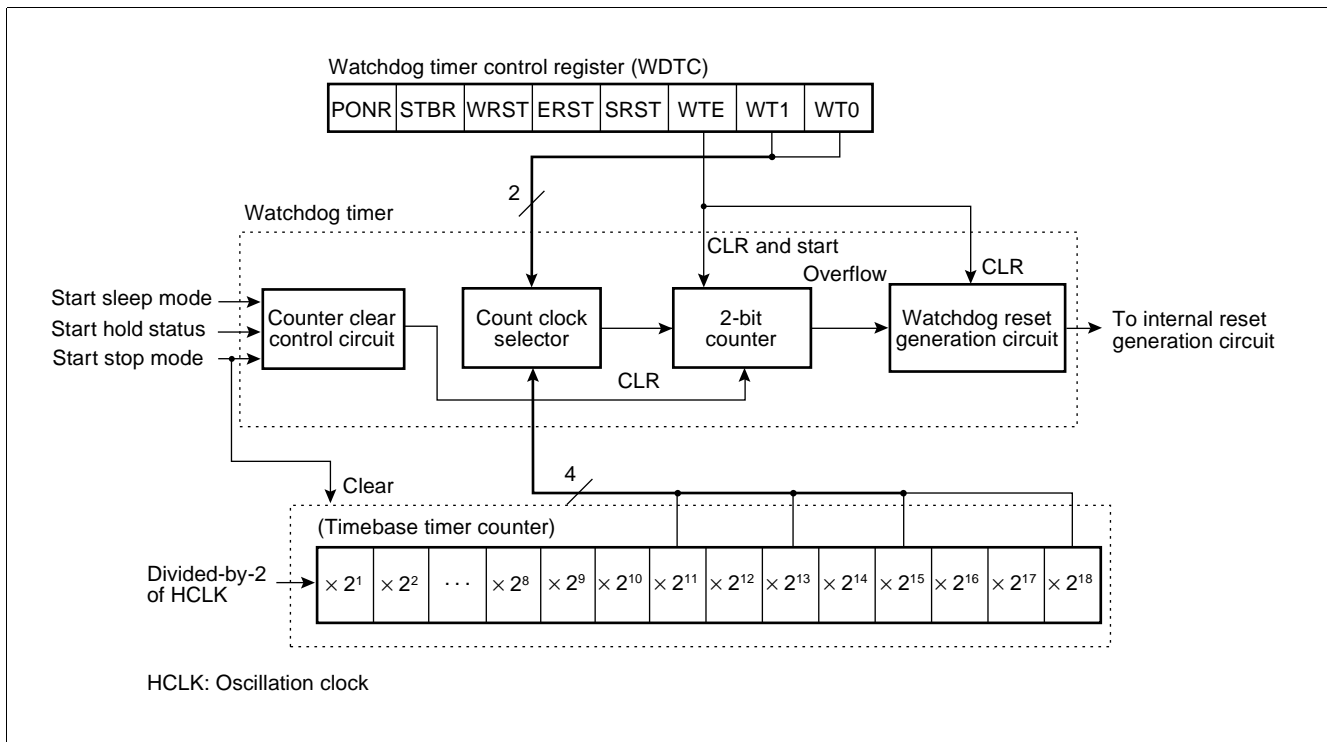
The watchdog timer is a 2-bit counter operating with an output of the timebase timer and resets the CPU when the counter is not cleared for a preset period of time.

(1) Register Configuration

- Watchdog timer control register (WDTC)



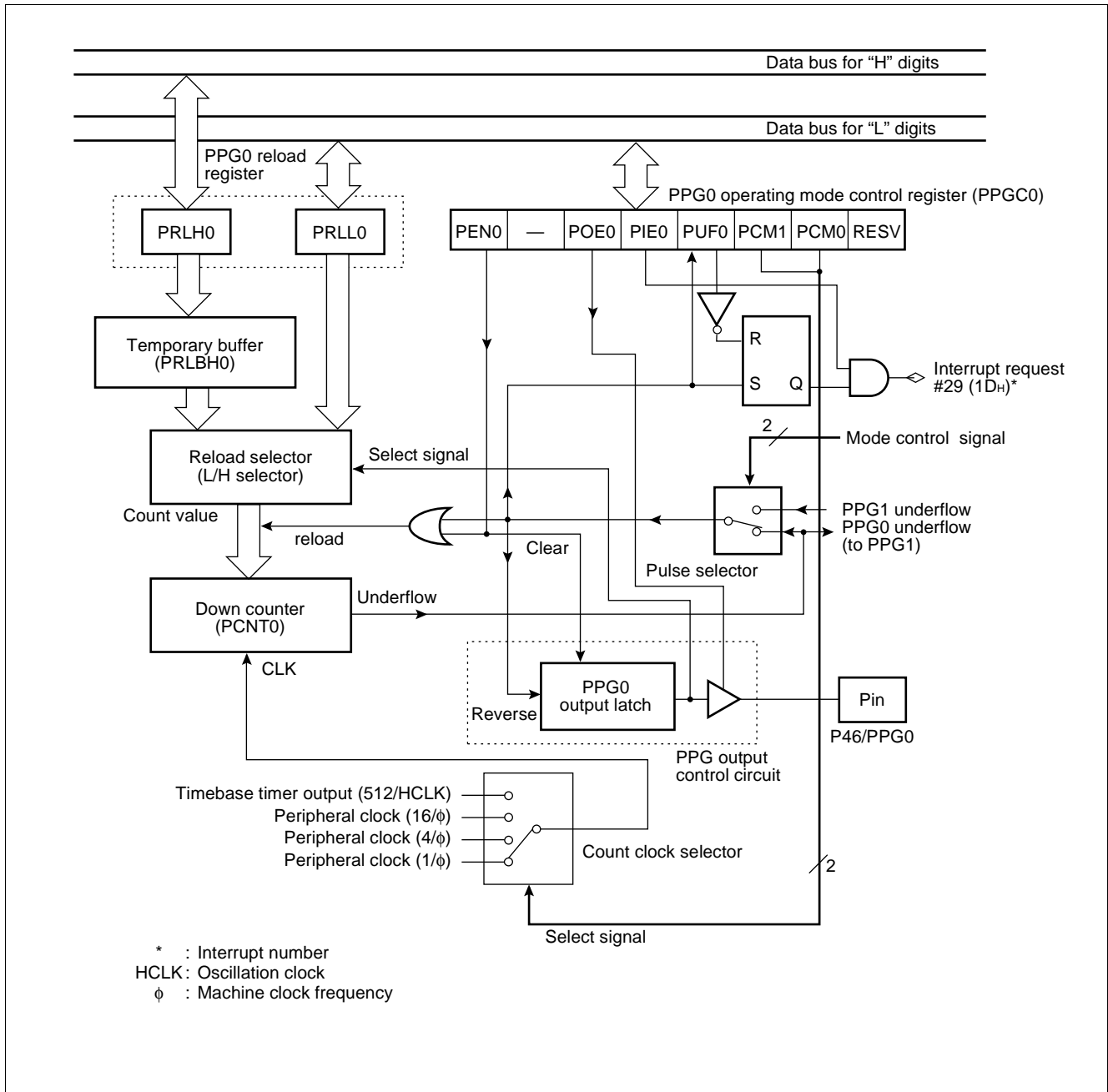
(2) Block Diagram



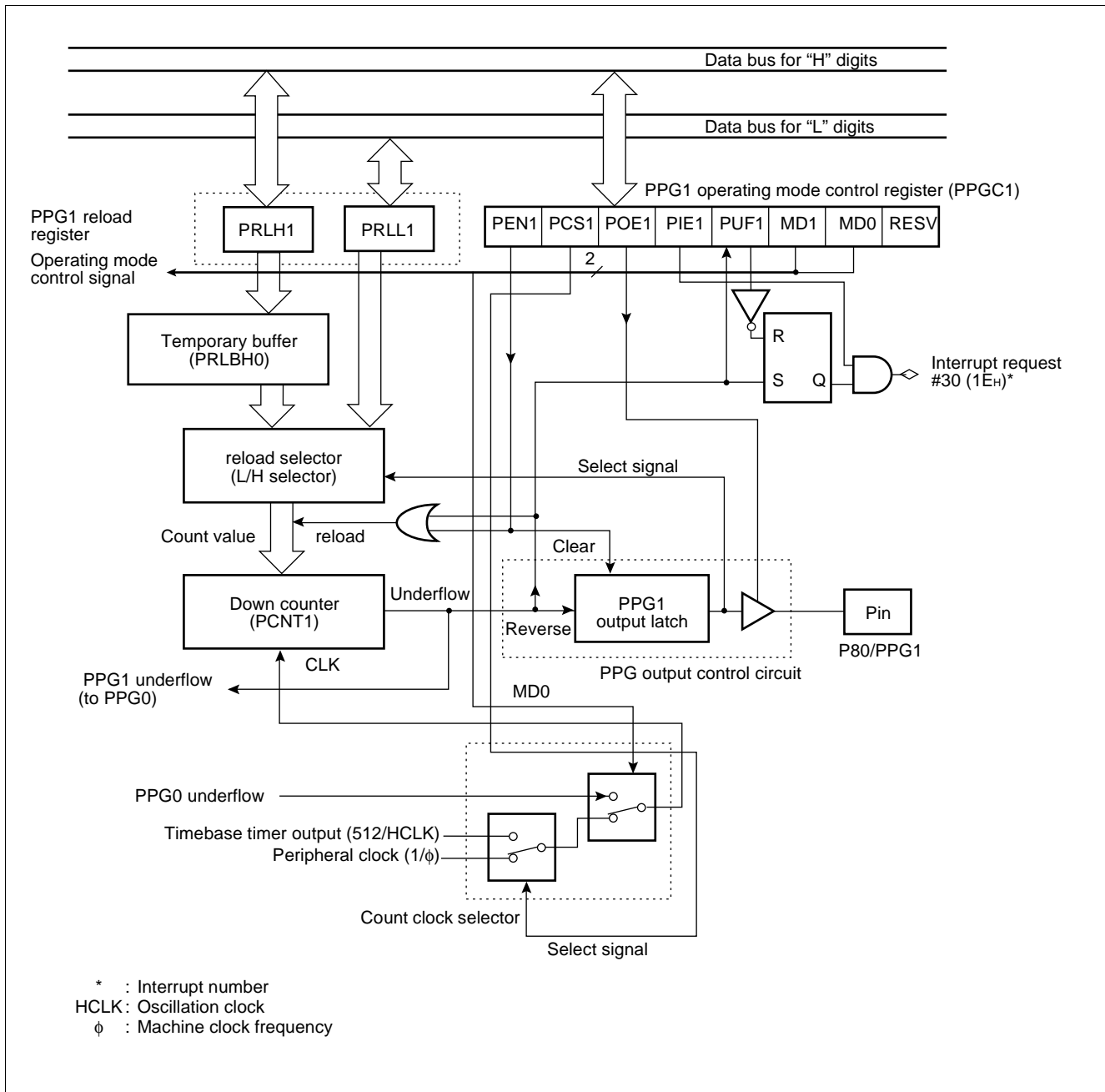
MB90670/675 Series

(2) Block Diagram

- Block diagram of 8/16-bit PPG timer 0



• Block diagram of 8/16-bit PPG timer 1



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5. 16-bit Reload Timer

The 16-bit reload timer has an internal clock mode for counting down in synchronization to three types of internal clocks and an event count mode for counting down detecting a given edge of the pulse input to the external bus pin, and either of the two functions can be selectively used.

For this timer, an “underflow” is defined as the counter value of “0000H” to “FFFFH”. According to this definition, an underflow occurs after [reload register setting value + 1] counts.

In operating the counter, the reload mode for repeating counting operation after reloading a counter setting value after an underflow or the one-shot mode for stopping the counting operation after an underflow can be selectively used.

Because the timer can generate an interrupt upon an underflow, the timer conforms to the extended intelligent I/O service (EI²OS).

The MB90670/675 series has 2 channels of 16-bit reload timers.

(1) Register Configuration

- Timer control status register upper digits (TMCSR0, TMCSR1 : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
TMCSR0:000039H TMCSR1:00003DH	—	—	—	—	CSL1	CSL0	MOD2	MOD1	(TMCSR : L)			----0000B
	—	—	—	—	R/W	R/W	R/W	R/W				

- Timer control status register lower digits (TMCSR0, TMCSR1 : L)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
TMCSR0:000038H TMCSR1:00003CH	(TMCSR : H)			MOD1	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	00000000B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- 16-bit timer register 0, 1 (TMR0, TMR1)

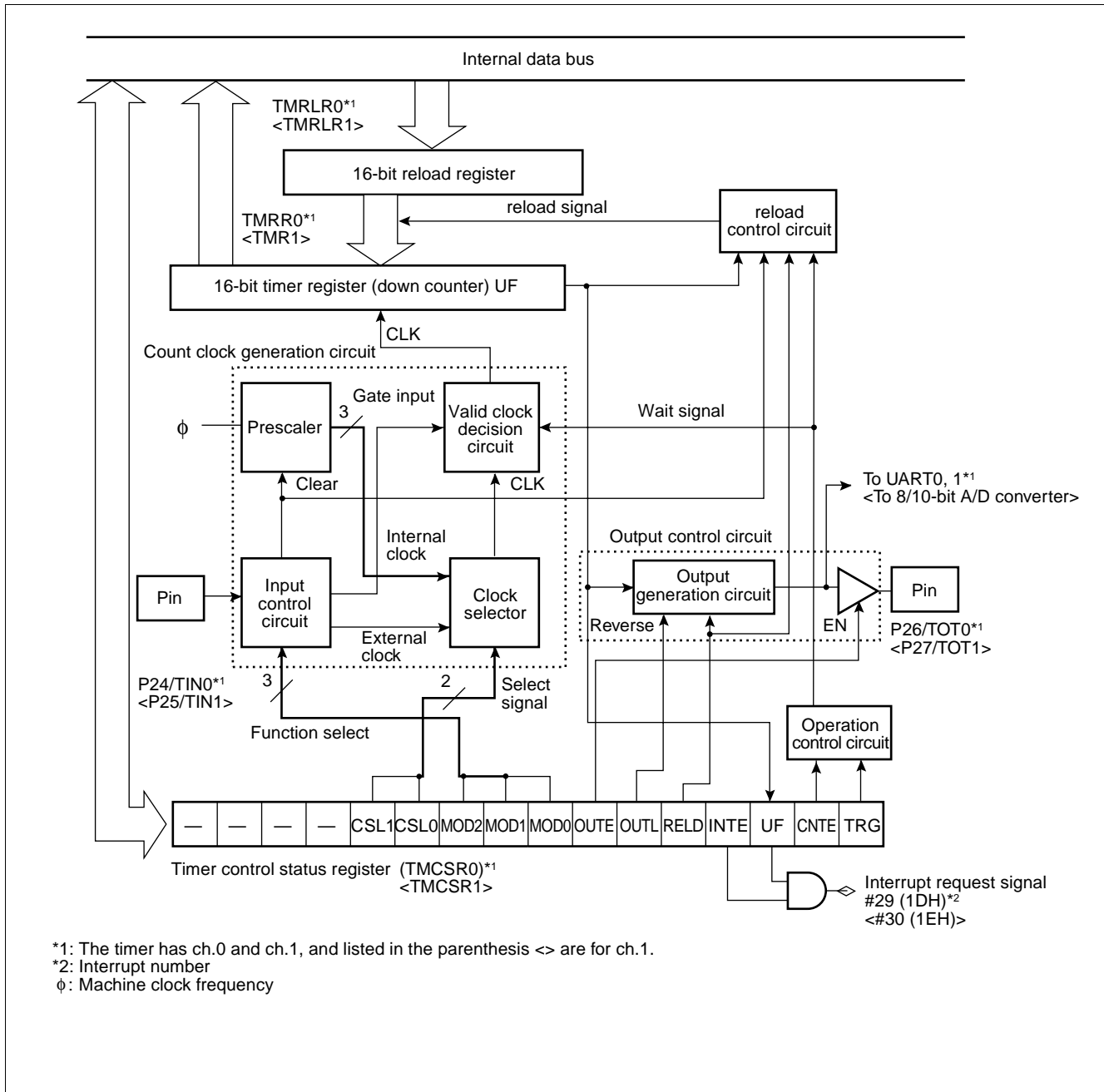
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003AH 00003BH 00003EH 00003FH																	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

- 16-bit reload register 0, 1 (TMRL0, TMRL1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00003AH 00003BH 00003EH 00003FH																	XXXXXXXXB XXXXXXXXB XXXXXXXXB XXXXXXXXB
	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	

R/W : Readable and writable
 R : Read only
 W : Write only
 — : Unused
 X : Indeterminate

(2) Block Diagram



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6. 24-bit Free-run Timer

The 24-bit free-run timer is a 24-bit up counter for counting up in synchronization to divided-by-3 or divided-by-4 of the machine clock, in which an interrupt factor can be selected from the overflow interrupt and four types of timer intermediate bit interrupt to be operated as an interval timer.

The free-run timer can be used to generating reference timing signals for the input capture (ICU) and output compare (OCU).

(1) Register Configuration

- Free-run timer control register upper digits (TCCR : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000051 _H	—	—	RESV	RESV	RESV	RESV	RESV	PR0	(TCCR : L)			--111111 _B
	—	—	R/W	R/W	R/W	R/W	R/W	R/W				

- Free-run timer control register lower digits (TCCR : L)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000050 _H	(TCCR : H)			STP	CLR	IVF	IVFE	TIM	TIME	TIS1	TIS0	11000000 _B
				W	W	R/W	R/W	R/W	R/W	R/W	R/W	

- Free-run timer upper data register (TCRH)

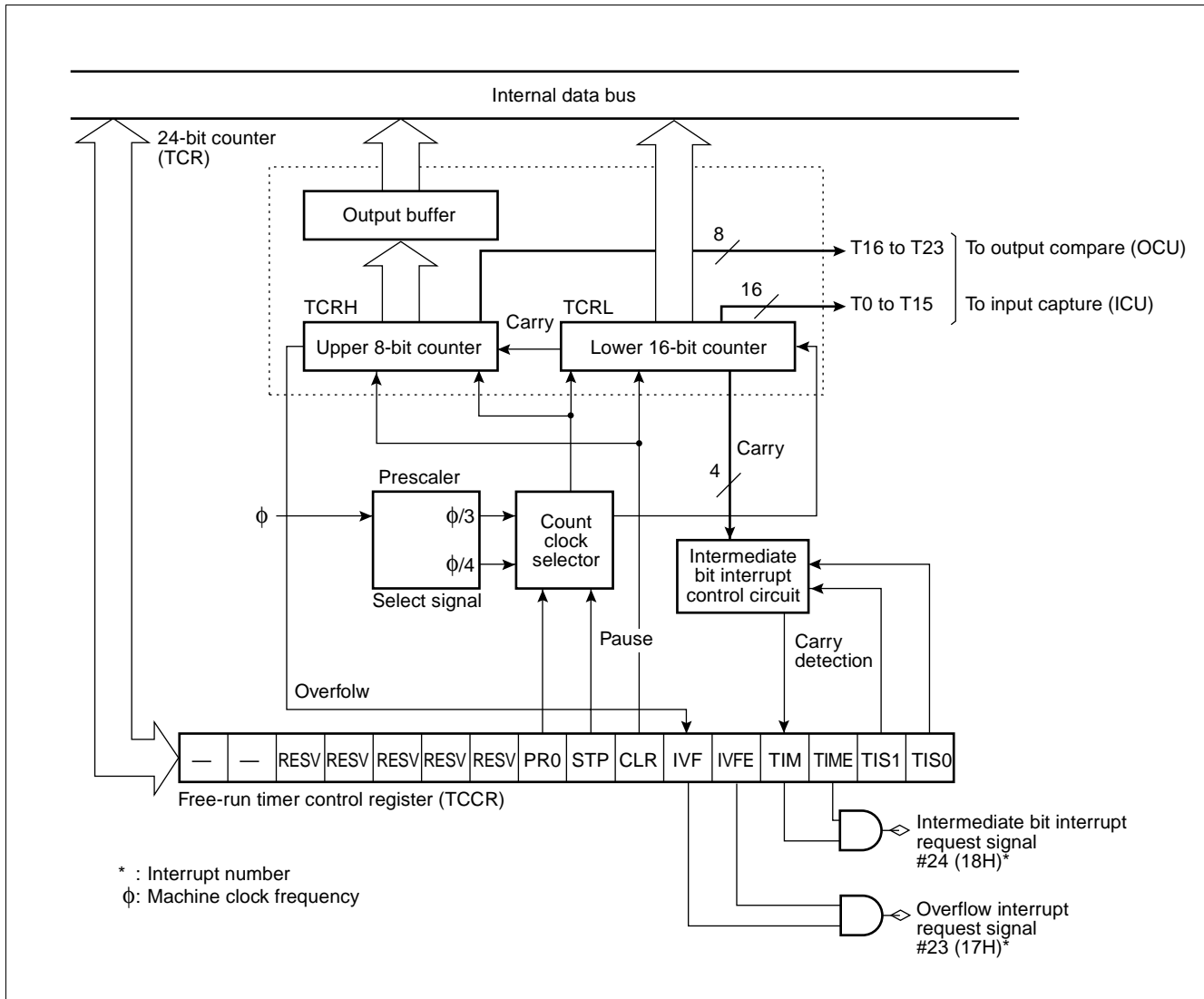
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000056 _H 000057 _H	—	—	—	—	—	—	—	—	T23	T22	T21	T20	T19	T18	T17	T16	00000000 _B 00000000 _B
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

- Free-run timer lower data register (TCRL)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000054 _H 000055 _H	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	00000000 _B 00000000 _B
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

R/W : Readable and writable
 R : Read only
 W : Write only
 — : Unused

(2) Block Diagram



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7. Input Capture (ICU)

The input capture (ICU) generates an interrupt request to the CPU simultaneously with a storing operation of current counter value of the 24-bit free-run timer to the ICU data register (ICDR) upon an input of a trigger edge to the external pin.

There are four sets (four channels) of the input capture external pins and ICU data registers (ICDR), enabling measurements of maximum of four events.

- The input capture has four sets of external input pins (ASR0 to ASR3) and ICU registers (ICDR), enabling measurements of maximum of four events.
- A trigger edge direction can be selected from rising/falling/both edges.
- The input capture can be set to generate an interrupt request at the storage timing of the counter value of the 24-bit free-run timer to the ICU data register (ICDR).
- The input compare conforms to the extended intelligent I/O service (EI²OS).
- The input capture function is suited for measurements of intervals (frequencies) and pulse-widths.

(1) Register Configuration

- ICU control register upper digits (ICC : H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7..... bit 0	Initial value
000053 _H	IRE3	IRE2	IRE1	IRE0	IR3	IR2	IR1	IR0	(ICC : L)	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

- ICU control register lower digits (ICC : L)

Address	bit 15..... bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000052 _H	(ICC : H)	EG3B	EG3A	EG2B	EG2A	EG1B	EG1A	EG0B	EG0A	00000000 _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- ICU upper data register 0 to 3 (ICDR0H to ICDR3H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ICDR0H : 000063 _H ICDR1H : 000067 _H ICDR2H : 00006B _H ICDR3H : 00006F _H	—	—	—	—	—	—	—	—	00000000 _B
	R	R	R	R	R	R	R	R	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ICDR0H : 000062 _H ICDR1H : 000066 _H ICDR2H : 00006A _H ICDR3H : 00006E _H	D23	D22	D21	D20	D19	D18	D17	D16	XXXXXXXX _B
	R	R	R	R	R	R	R	R	

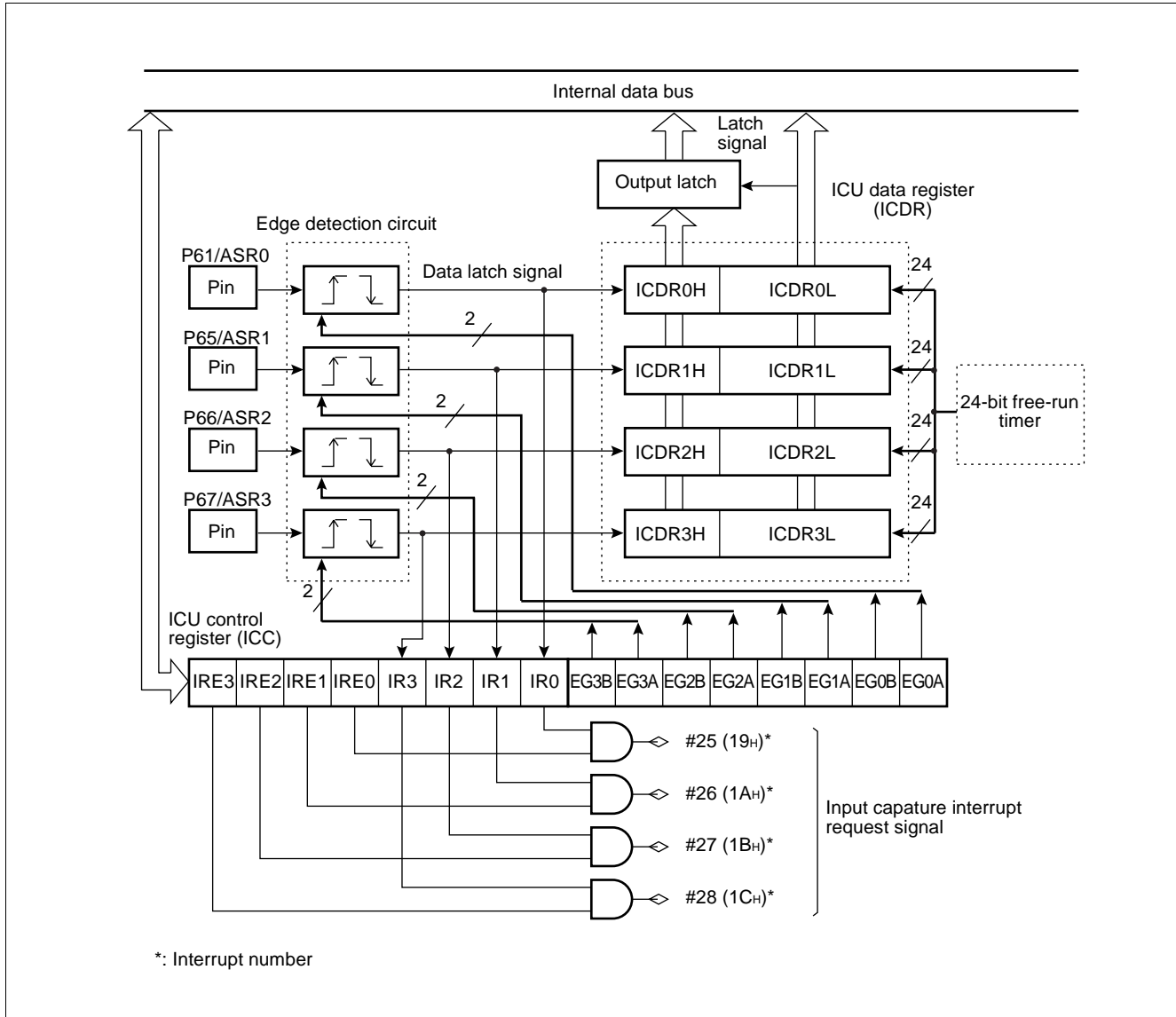
- ICU lower data register 0 to 3 (ICDR0L to ICDR3L)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
ICDR0L : 000061 _H ICDR1L : 000065 _H ICDR2L : 000069 _H ICDR3L : 00006D _H	D15	D14	D13	D12	D11	D10	D9	D8	XXXXXXXX _B
	R	R	R	R	R	R	R	R	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
ICDR0L : 000060 _H ICDR1L : 000064 _H ICDR2L : 000068 _H ICDR3L : 00006C _H	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
	R	R	R	R	R	R	R	R	

R/W : Readable and writable
 R : Read only
 — : Unused
 X : Indeterminate

(2) Block Diagram



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8. Output Compare (OCU)

The output compare (OCU) is two sets of compare units consisting of four-channel OCU compare data registers, a comparator and a control register.

An interrupt request can be generated for each channel upon a match detection by performing time-division comparison between the OCU compare data register setting value and the counter value of the 24-bit free-run timer.

The DOT pin can be used as a waveform output pin for reversing output upon a match detection or a general-purpose output port for directly outputting the setting value of the DOT bit.

(1) Register Configuration

• OCU control register 00 upper digits (CCR00 : H)											
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....	bit 0	Initial value
000059H	—	—	—	—	MD3	MD2	MD1	MD0	(CCR00 : L)		----0000 _B
					R/W	R/W	R/W	R/W			
• OCU control register 00 lower digits (CCR00 : L)											
Address	bit 15.....	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000058H	(CCR00 : H)		RESV	RESV	RESV	RESV	CPE3	CPE2	CPE1	CPE0	11110000 _B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
• OCU control register 01 upper digits (CCR01 : H)											
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....	bit 0	Initial value
00005BH	ICE3	ICE2	ICE1	ICE0	IC3	IC2	IC1	IC0	(CCR01 : L)		00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
• OCU control register 01 lower digits (CCR01 : L)											
Address	bit 15.....	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00005AH	(CCR01 : H)		—	—	—	—	DOT3	DOT2	DOT1	DOT0	----0000 _B
							R/W	R/W	R/W	R/W	
R/W : Readable and writable — : Unused											

(Continued)

(Continued)

- OCU compare upper data register 0 to 7 (CPR00H to CPR07H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
CPR00H : 000073H	—	—	—	—	—	—	—	—	00000000 _B
CPR01H : 000077H									
CPR02H : 00007BH									
CPR03H : 00007FH									
CPR04H : 000083H									
CPR05H : 000087H									
CPR06H : 00008BH									
CPR07H : 00008FH									

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
CPR00H : 000072H	D23	D22	D21	D20	D19	D18	D17	D16	00000000 _B
CPR01H : 000076H									
CPR02H : 00007AH									
CPR03H : 00007EH									
CPR04H : 000082H									
CPR05H : 000086H									
CPR06H : 00008AH									
CPR07H : 00008EH									

- OCU compare lower data register 0 to 7 (CPR00L to CPR07L)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Initial value
CPR00L : 000071H	D15	D14	D13	D12	D11	D10	D9	D8	00000000 _B
CPR01L : 000075H									
CPR02L : 000079H									
CPR03L : 00007DH									
CPR04L : 000081H									
CPR05L : 000085H									
CPR06L : 000089H									
CPR07L : 00008DH									

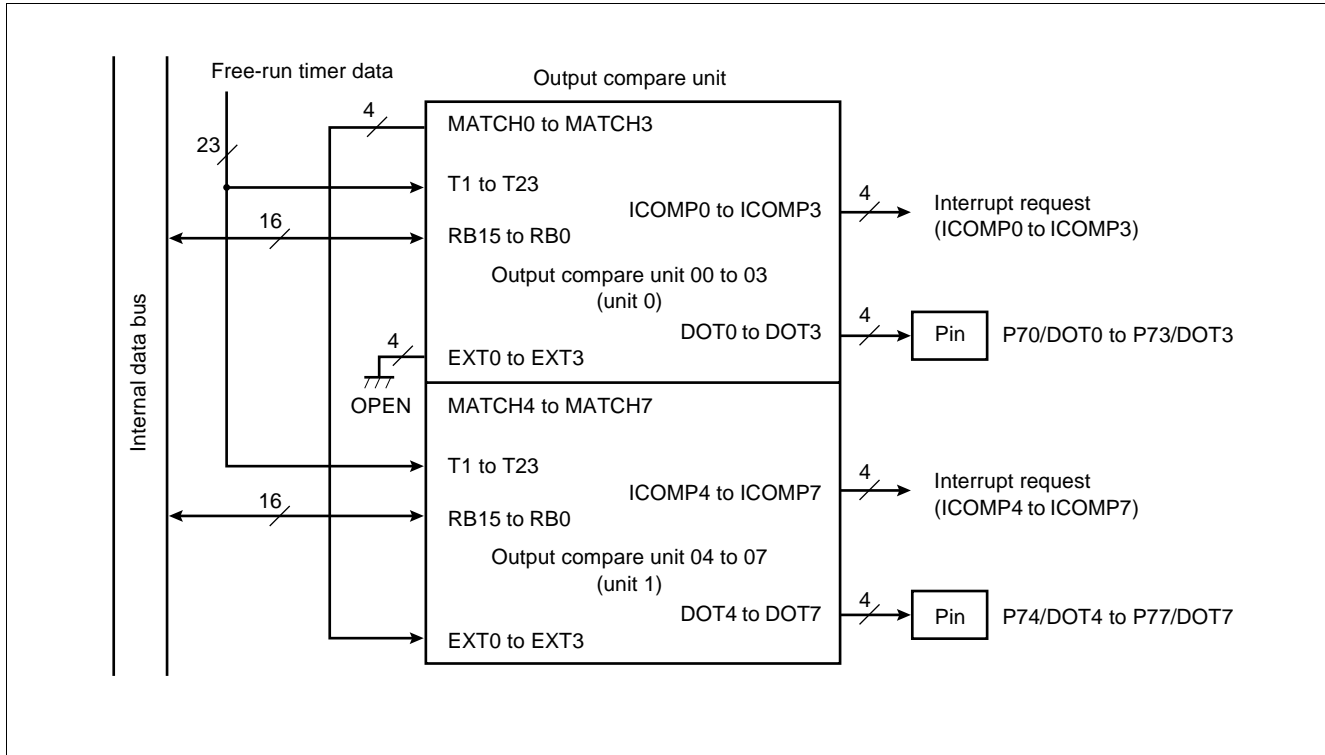
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
CPR00L : 000070H	D7	D6	D5	D4	D3	D2	D1	D0	00000000 _B
CPR01L : 000074H									
CPR02L : 000078H									
CPR03L : 00007CH									
CPR04L : 000080H									
CPR05L : 000084H									
CPR06L : 000088H									
CPR07L : 00008CH									

R/W : Readable and writable
 — : Unused

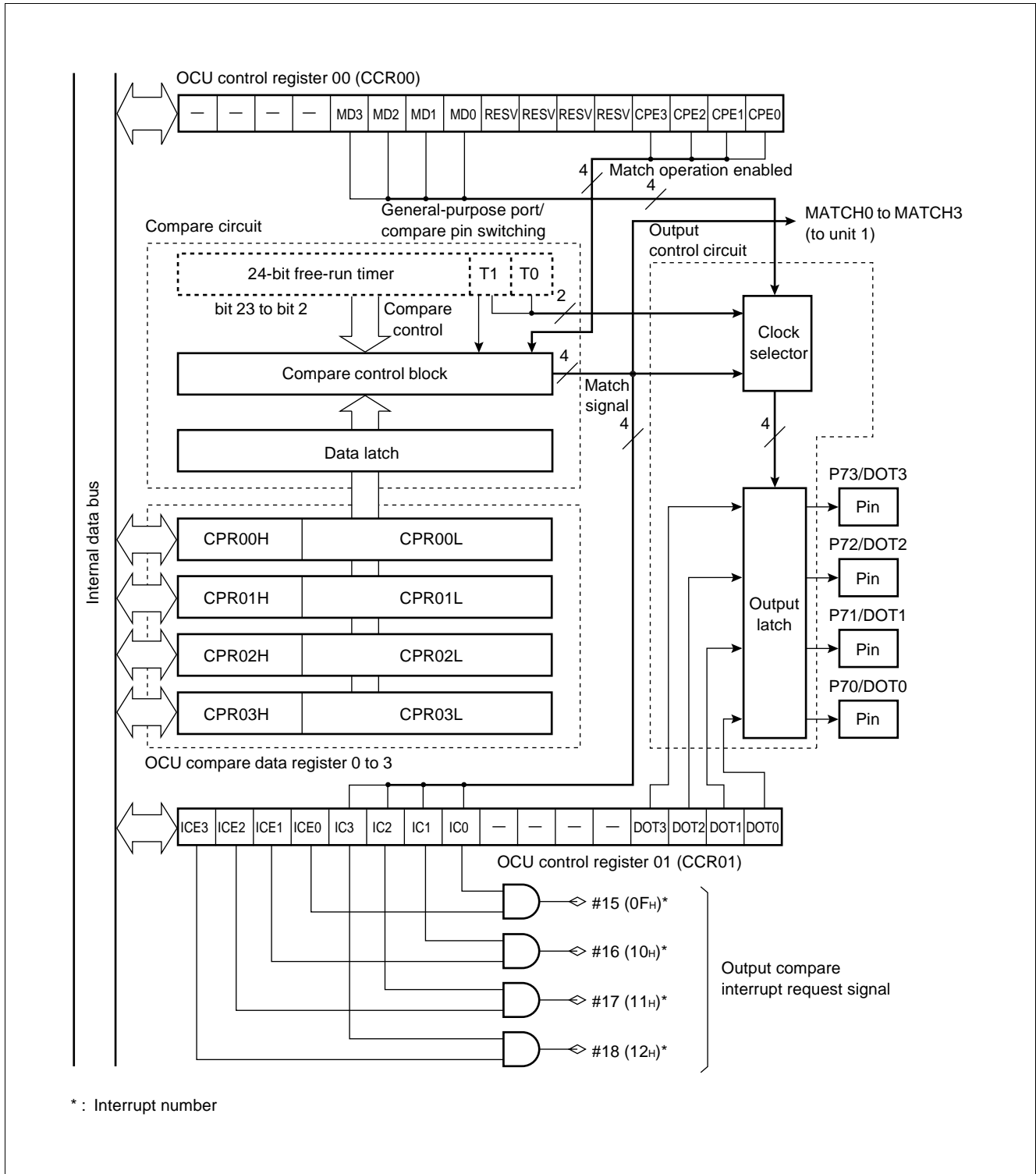
MB90670/675 Series

(2) Block Diagram of Output Compare (OCU)

• Overall block diagram

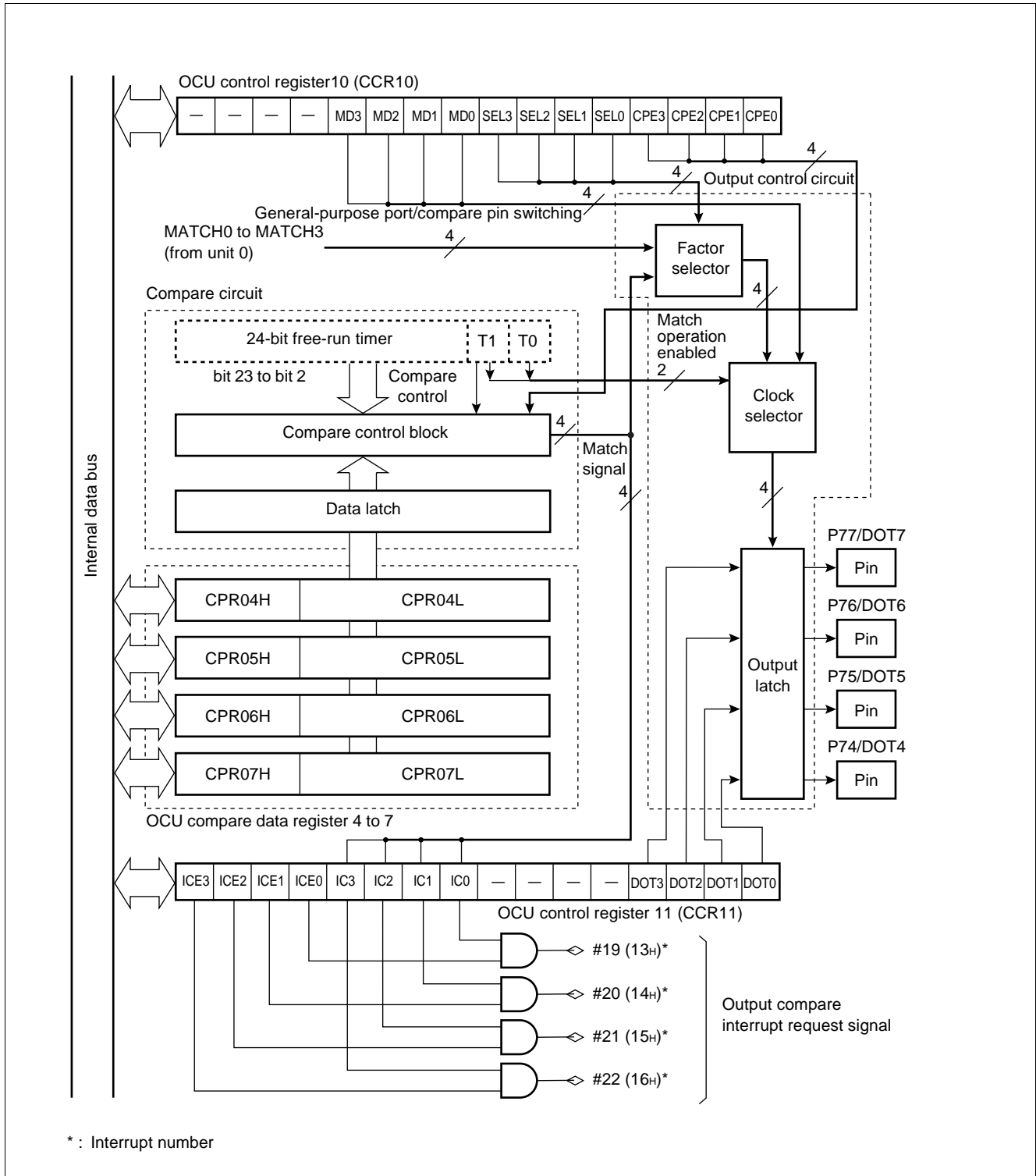


• Block diagram of unit 0



MB90670/675 Series

• Block diagram of unit 1



9. I²C Interface (Included Only in MB90675 Series)

The I²C interface is a serial I/O port supporting Inter IC BUS operating as master/slave devices on I²C bus and has the following features.

- Master/slave transmission/reception
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transmission direction detection function
- Repeated generation function start condition and detection function
- Bus error detection function

(1) Register Configuration

• I²C bus status register (IBSR)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000040 _H	(IBSR)		BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	0000000 _B
			R	R	R	R	R	R	R	R	

• I²C bus control register (IBCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000041 _H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	(IBSR)		0000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

• I²C bus clock control register (ICCR)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000042 _H	(IADR)		—	—	EN	CS4	CS3	CS2	CS1	CS0	--0XXXX _B
			—	—	R/W	R/W	R/W	R/W	R/W	R/W	

• I²C address register (IADR)

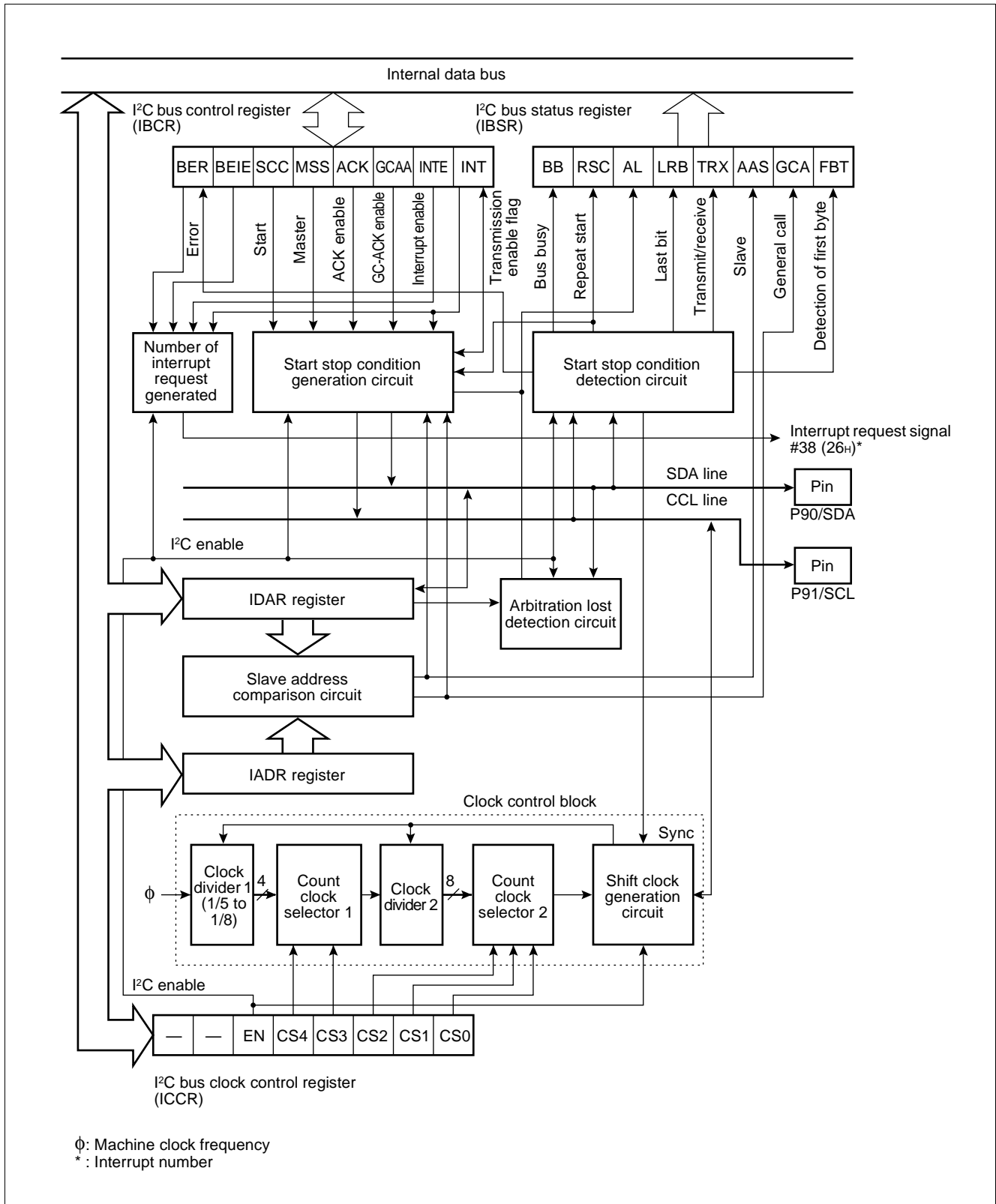
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000043 _H (IADR)	—	A6	A5	A4	A3	A2	A1	A0	(ICCR)		-XXXXXXX _B
	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000044 _H (IDAR)	(Reserved area)		D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 R : Read only
 — : Unused
 X : Indeterminate

MB90670/675 Series

(2) Block Diagram



10. UART0

UART0 is a general-purpose serial data communication interface for performing synchronous or asynchronous communication (start-stop synchronization system). In addition to the normal duplex communication function (normal mode), UART0 has a master/slave type communication function (multi-processor mode).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (with start and stop bit)
Clock asynchronous (start-stop synchronization system)
- Baud rate: With dedicated baud rate generator, selectable from 12 types
External clock input possible
Internal clock (a clock supplied from 16-bit reload timer can be used.)
- Data length: 7 bits to 9 bits selective (with a parity bit)
6 bits to 8 bits selective (without a parity bit)
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
Overrun error
Parity error (not available in multi-processor mode)
- Interrupt request: Receive interrupt (reception complete, receive error detection)
Receive interrupt (transmission complete)
Transmit/receive conforms to extended intelligent I/O service (EI²OS)
- Master/slave type communication function (multi-processor mode): 1 (master) to n (slave) communication possible

(1) Register Configuration

• Status register 0 (USR0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....bit 0	Initial value
000021 _H	RDRF	ORFE	PE	TDRE	RIE	TIE	RBF	TBF	(UMC0)	00100000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

• Mode control register 0 (UMC0)

Address	bit 15.....bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000020 _H	(USR0)	PEN	SBL	MC1	MC0	SMDE	RFC	SCKE	SOE	00000100 _B
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

• Rate and data register 0 (URD0)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7.....bit 0	Initial value
000023 _H	BCH	RC3	RC2	RC1	RC0	BCH0	P	D8	(UIDR0/UODR0)	00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

• Input data register 0 (UIDR0)

Address	bit 15.....bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022 _H	(URD0)	D8	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
		R	R	R	R	R	R	R	R	R	

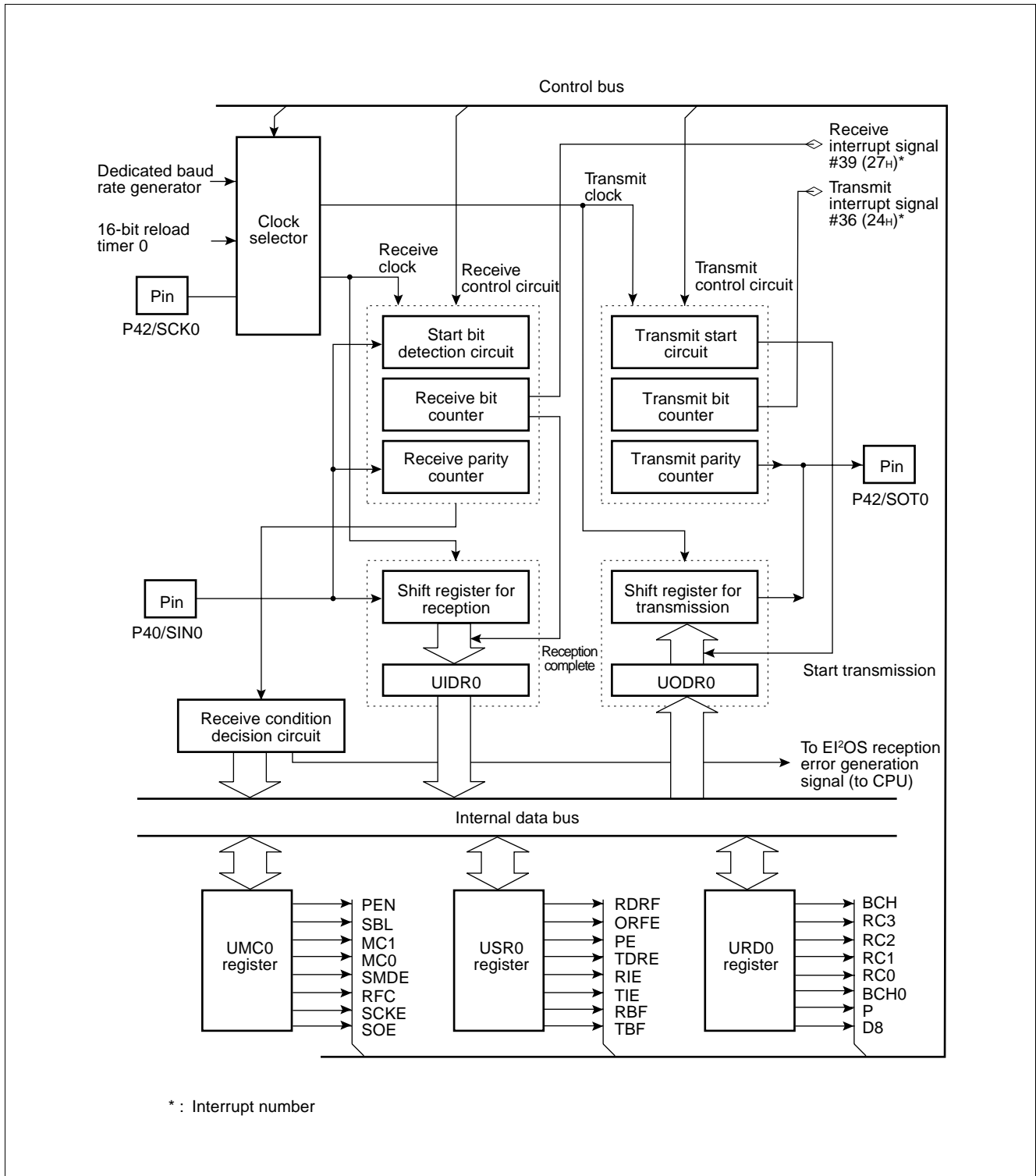
• Output data register 0 (UODR)

Address	bit 15.....bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000022 _H	(URD0)	D8	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
		W	W	W	W	W	W	W	W	W	

R/W : Readable and writable
R : Read only
W : Write only
X : Indeterminate

MB90670/675 Series

(2) Block Diagram



11. UART1 (SCI)

UART1 (SCI) is a general-purpose serial data communication interface for performing synchronous or asynchronous communication (start-stop synchronization system). In addition to the normal duplex communication function (normal mode), UART1 has a master-slave type communication function (multi-processor mode).

- Data buffer: Full-duplex double buffer
- Transfer mode: Clock synchronized (no start or stop bit)
Clock asynchronous (start-stop synchronization system)
- Baud rate: With dedicated baud rate generator, selectable from 8 types
External clock input possible
Internal clock (a internal clock supplied from 16-bit reload timer can be used.)
- Data length: 7 bits (for asynchronous normal mode only)
8 bits
- Signal format: NRZ (Non Return to Zero) system
- Reception error detection: Framing error
Overrun error
Parity error (not available in multi-processor mode)
- Interrupt request: Receive interrupt (receptioncomplete, receive error detection)
Receive interrupt (transmission complete)
Transmit/receive conforms to extended intelligent I/O service (EI²OS)
- Master/slave type communication function (multi-processor mode): 1 (master) to n (slave) communication possible (supported only for master station)

(1) Register Configuration

- Control register 1 (SCR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000025 _H	PEN	P	SBL	CL	A/D	REC	RXE	TXE	(SMR1)			00000100 _B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

- Mode register 1 (SMR1)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000024 _H	(SCR1)			MD1	MD0	CS2	CS1	CS0	BCH	SCKE	SOE	00000000 _B
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Status register 1 (SSR1)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000027 _H	PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	(SIDR1/SODR1)			00001-00 _B
	R	R	R	R	R	—	R/W	R/W				

- Input data register 1 (SIDR1)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000026 _H	(SSR1)			D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
			R	R	R	R	R	R	R	R	R	

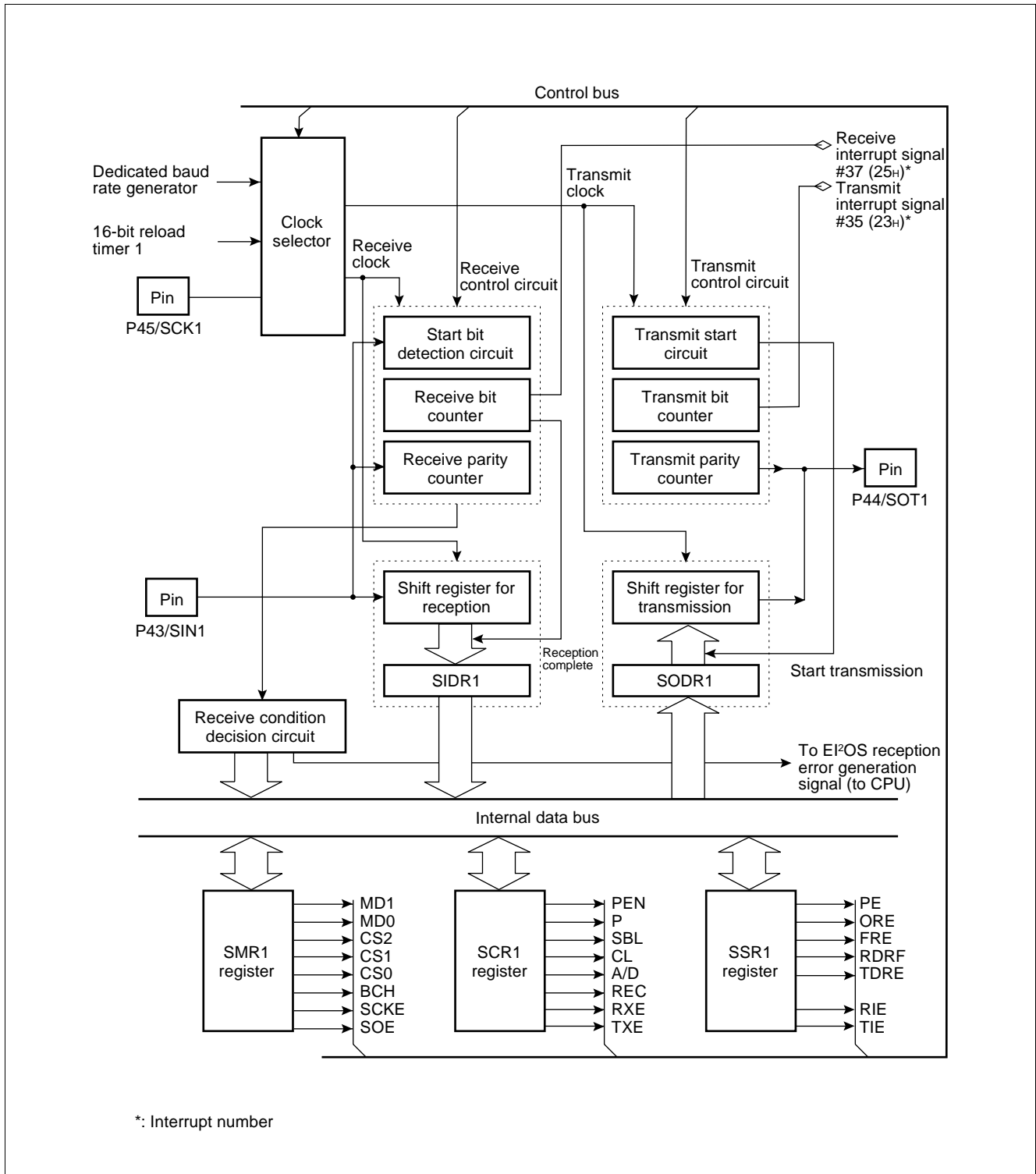
- Output data register 1 (SODR1)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000026 _H	(SSR1)			D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B
			W	W	W	W	W	W	W	W	W	

R/W: Readable and writable
 R : Read only
 W : Write only
 — : Unused
 X : Indeterminate

MB90670/675 Series

(2) Block Diagram



12. DTP/External Interrupt Circuit

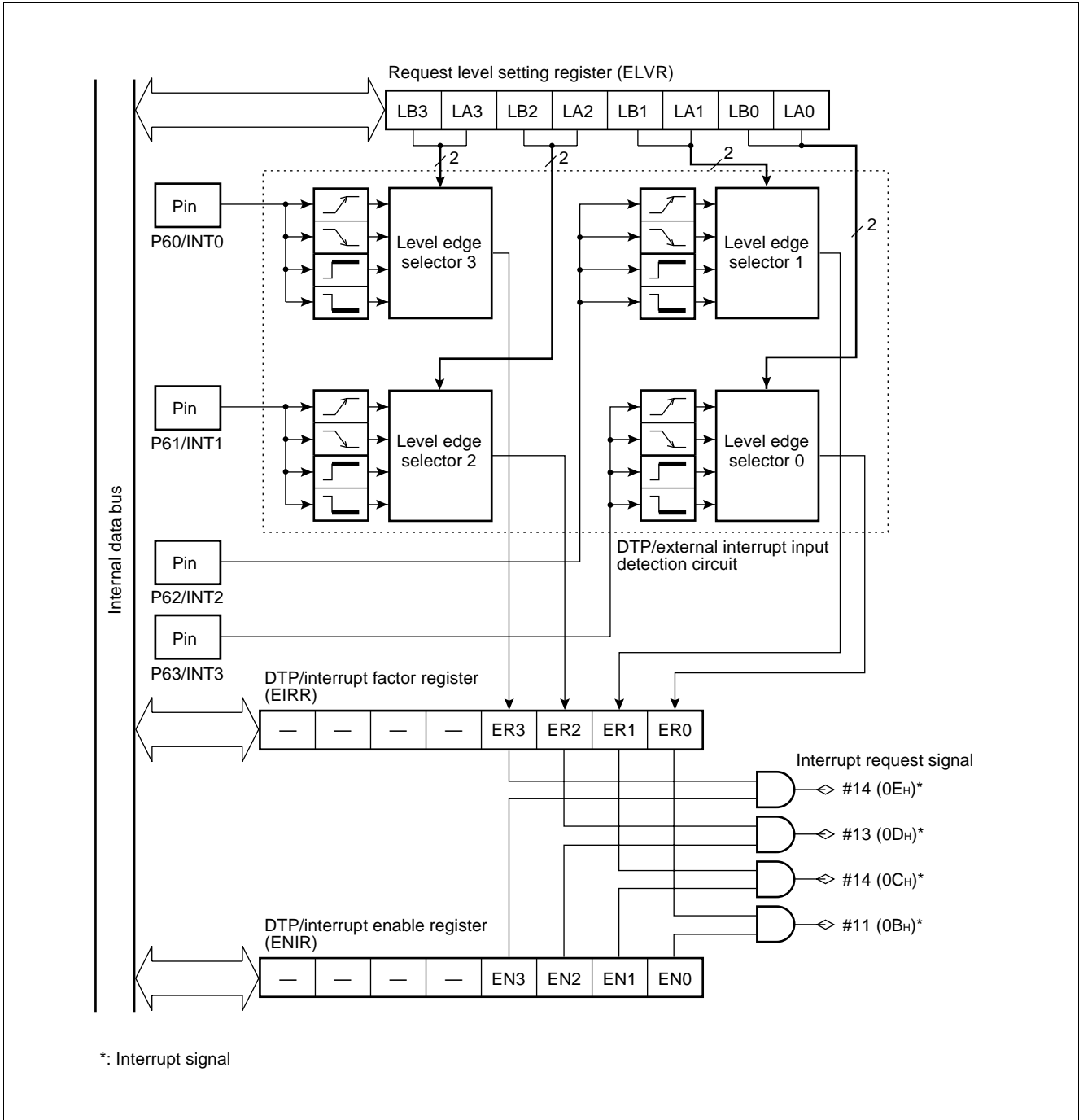
The DTP (Data Transfer Peripheral)/external interrupt circuit is located between peripheral equipment connected externally and the F²MC-16L CPU and transmits interrupt requests or data transfer requests generated by peripheral equipment to the CPU, generates external interrupt request and starts the extended intelligent I/O service (EI²OS).

(1) Register Configuration

• DTP/interrupt factor register (EIRR)												
Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
000029 _H	—	—	—	—	ER3	ER2	ER1	ER0	(ENIR)			----0000 _B
	—	—	—	—	R/W	R/W	R/W	R/W				
• DTP/interrupt enable register (ENIR)												
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
000028 _H	(EIRR)			—	—	—	—	EN3	EN2	EN1	EN0	----0000 _B
				—	—	—	—	R/W	R/W	R/W	R/W	
• Request level setting register (ELVR)												
Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00002A _H	(Vacancy)			LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
R/W: Readable and writable — : Unused												

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(2) Block Diagram



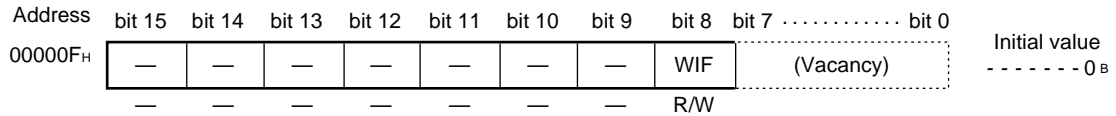
13. Wake-up Interrupt

Wake-up interrupts transmits interrupt request ("L" level) generated by peripheral device located between external peripheral devices and the F²MC-16L CPU to the CPU and invokes interrupt processing.

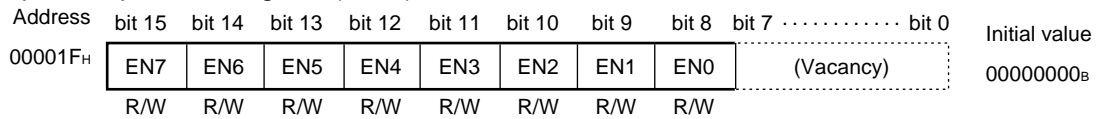
The interrupt does not conform to the extended intelligent I/O service (EI²OS).

(1) Register Configuration

- Wake-up interrupt flag register (EIFR)

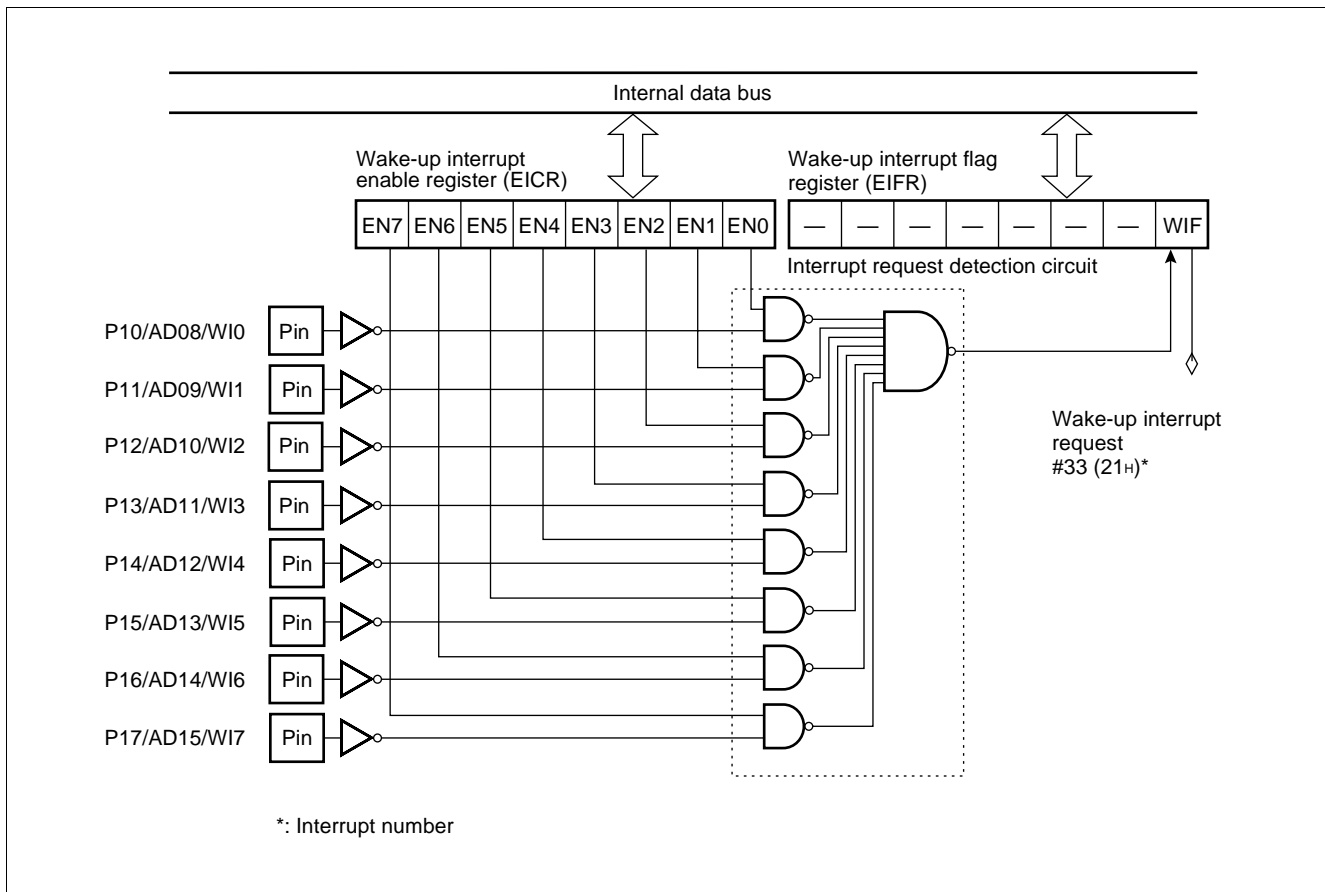


- Wake-up interrupt enable register (EICR)



R/W: Readable and writable
 — : Unused

(2) Block Diagram



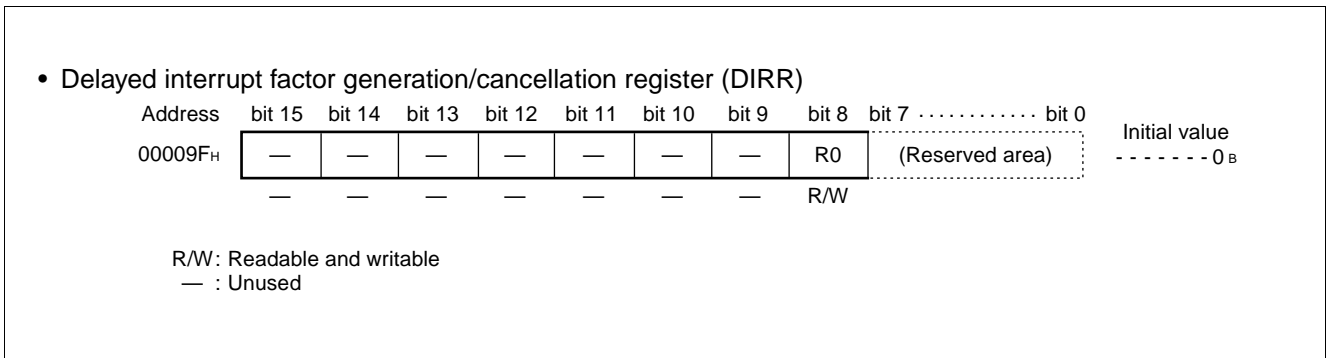
MB90670/675 Series

14. Delayed Interrupt Generation Module

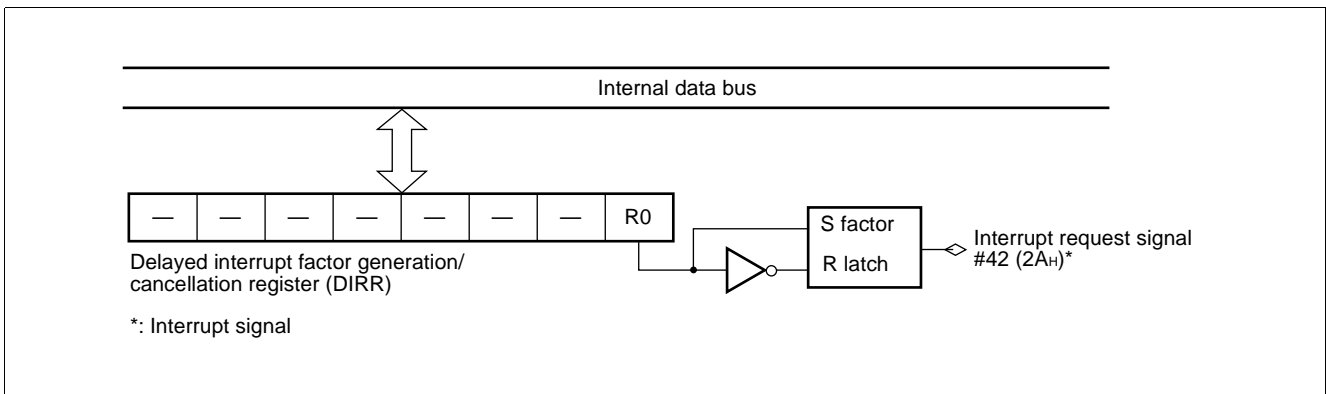
The delayed interrupt generation module generates interrupts for switching tasks for development on a real-time operating system (REALOS software). The module can be used to generate hardware interrupt requests to the CPU with software and cancel the interrupt requests.

This module does not conform to the extended intelligent I/O service (EI²OS).

(1) Register Configuration



(2) Block Diagram



15. 8/10-bit A/D Converter

The 8/10-bit A/D converter has a function of converting analog voltage input to the analog input pins (input voltage) to digital values (A/D conversion) and has the following features.

- Minimum conversion time: 6.13 μ s (at machine clock of 16 MHz, including sampling time)
- Minimum sampling time: 3.75 μ s (at machine clock of 16 MHz)
- Conversion method: RC successive approximation method with a sample and hold circuit.
- Resolution: 10-bit or 8-bit selective
- Analog input pins: Selectable from eight channels by software

One-shot conversion mode: Stops conversion after completing a conversion for a stopped channel (one channel only) or for successive channels (maximum of eight channels can be specified)

Continuous conversion mode: Continues conversions for a specified channel (one channel only) or for successive channels (maximum of eight channels can be specified)

Stop conversion mode: Stops conversion after completing a conversion for one channel and wait for the next activation.

- Interrupt requests can be generated and the extended intelligent I/O service (EI²OS) can be started after the end of A/D conversion.
- When interrupts are enabled, there is no loss of data even in continuous operations because the conversion data protection function is in effect.
- Starting factors for conversion: Selected from software activation, 16-bit reload timer 1 output (rising edge), and external trigger (falling edge).

(1) Register Configuration

- A/D control status register upper digits (ADCS: H)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
00002D _H	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	RESV	(ADCS: L)			00000000 _B
	R/W	R/W	R/W	R/W	R/W	R/W	W	R/W				

- A/D control status register lower digits (ADCS: L)

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00002C _H	(ADCS: H)			MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	00000000 _B
				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

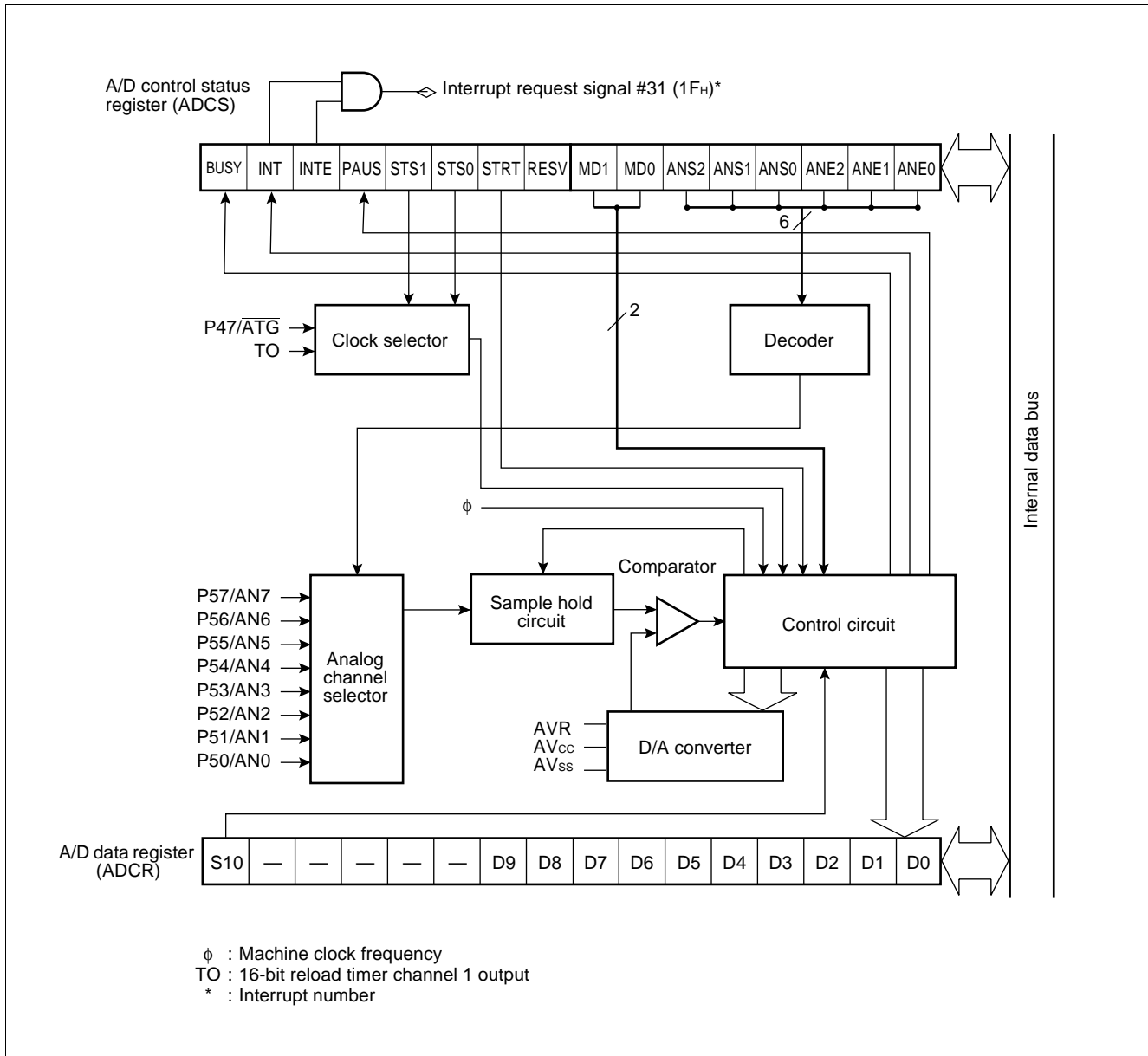
- A/D data register (ADCR)

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00002E _H	S10	—	—	—	—	—	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX _B 0000000X _B
	R/W	—	—	—	—	—	R	R	R	R	R	R	R	R	R	R	

R/W: Readable and writable
 R : Read only
 W : Write only
 — : Unused
 X : Indeterminate

MB90670/675 Series

(2) Block Diagram



16. Low-power Consumption (Standby) Mode

The F²MC-16L has the following CPU operating mode configured by selection of an operating clock and clock operation control.

- **Clock mode**

PLL clock mode: A mode in which the CPU and peripheral equipment are driven by PLL-multiplied oscillation clock (HCLK).

Main clock mode: A mode in which the CPU and peripheral equipment are driven by divided-by-2 of the oscillation clock (HCLK).

The PLL multiplication circuits stops in the mainclock mode.

- **CPU intermittent operation mode**

The CPU intermittent operation mode is a mode for reducing power consumption by operating the CPU intermittently while external bus and peripheral functions are operated at a high-speed.

- **Hardware stand-by mode**

The hardware standby mode is a mode for reducing power consumption by stopping clock supply (sleep mode) to the CPU by the low-power consumption control circuit, stopping clock supplies to the CPU and peripheral functions (timebase timer mode), and stopping oscillation clock (stop mode, hardware standby mode).

Of these modes, modes other than the PLL clock mode are power consumption modes.

(1) Register Configuration

- **Clock select register (CKSCR)**

Address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 0	Initial value
0000A1 _H	RESV	MCM	WS1	WS0	RESV	MCS	CS1	CS0	(LPMCR)			11111100 _B
	R/W	R	R/W	R/W	R/W	R/W	W	R/W				

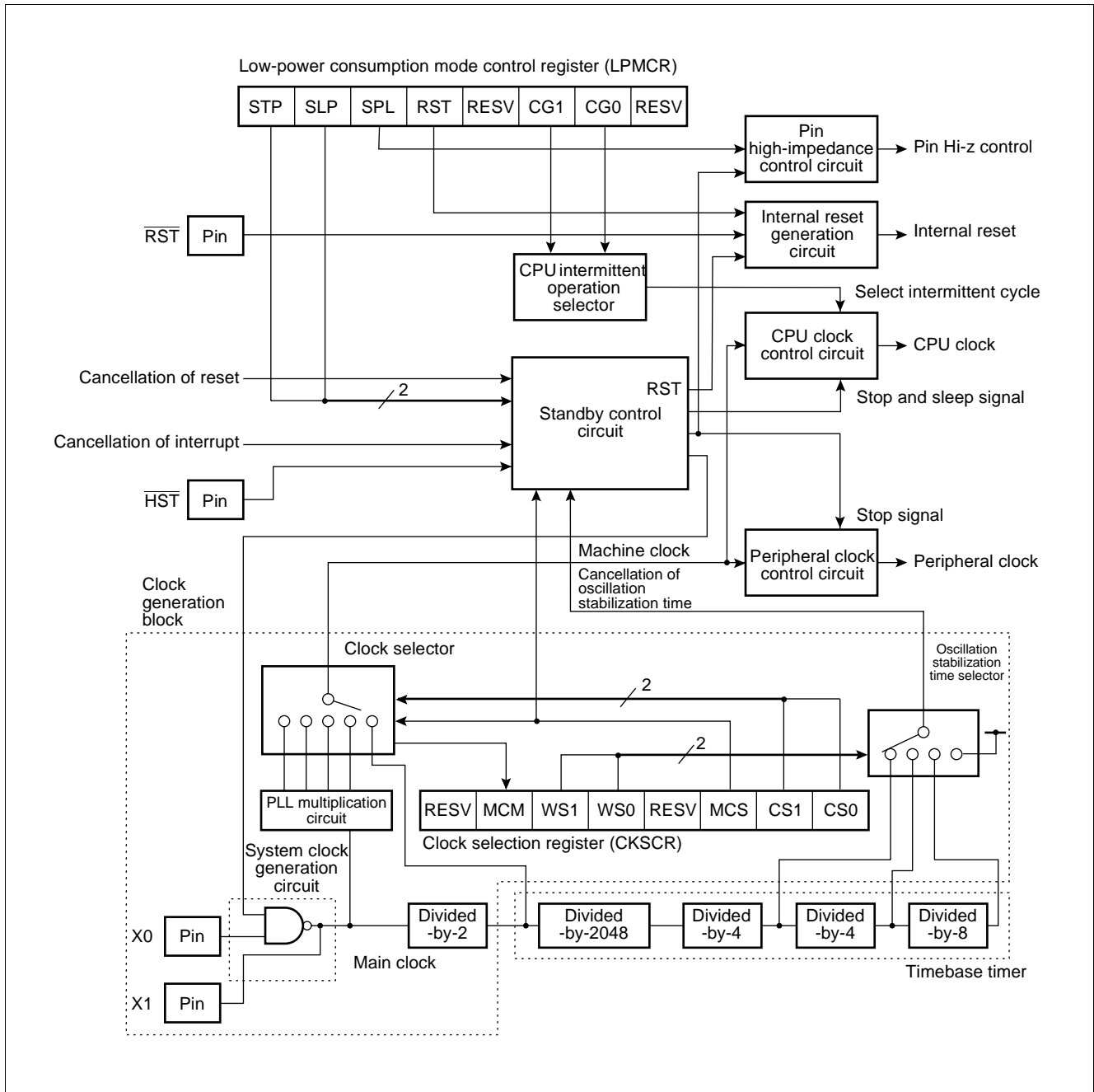
- **Low-power consumption mode control register (LPMCR)**

Address	bit 15	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0000A0 _H	(CKSCR)			STP	SLP	SPL	RST	RESV	CG1	CG0	RESV	00011000 _B
				W	W	R/W	W	R/W	R/W	R/W	R/W	

R/W: Readable and writable
 R : Read only
 W : Write only

MB90670/675 Series

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*1
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	*1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	*2
"L" level maximum output current	I_{OL}	—	15	mA	*3
"L" level average output current	I_{OLAV}	—	4	mA	*4
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	*5
"H" level maximum output current	I_{OH}	—	-15	mA	*3
"H" level average output current	I_{OHAV}	—	-4	mA	*4
"H" level total maximum output current	ΣI_{OH}	—	-100	mA	
"H" level total average output current	ΣI_{OHAV}	—	-50	mA	*5
Power consumption	P_D	—	400	mW	
Operating temperature	T_A	-40	+85	°C	
Storage temperature	T_{stg}	-55	+150	°C	

*1: AV_{CC} , AVRH, and AVRL shall never exceed V_{CC} . AVRL shall never exceed AVRH.

*2: V_I and V_O shall never exceed $V_{CC} + 0.3\text{ V}$.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90670/675 Series

2. Recommended Operating Conditions

($V_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.7	5.5	V	Normal operation
	V_{CC}	2.0	5.5	V	Retains status at the time of operation stop
Operating temperature	T_A	-40	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB90670/675 Series

3. DC Characteristics

($V_{CC} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	V_{IH}	Pins other than V_{IHS} and V_{IHM}	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80, HST, RST		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	MB90670 series
	V_{IHS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80 to P86, HST, RST, P90, P91, PA0 to PA7, PB0 to PB2		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	MB90675 series
	V_{IHM}	MD pin input		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	V_{IL}	Pins other than V_{ILS} and V_{ILM}	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	V_{ILS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80, HST, RST		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	MB90670 series
	V_{ILS}	Hysteresis input pins P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80 to P86, HST, RST, P90, P91, PA0 to PA7, PB0 to PB2		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	MB90675 series
	V_{ILM}	MD pin input		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
“H” level output voltage	V_{OH}	Other than P50 to P57	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	V_{OH}	Other than P50 to P57	$V_{CC} = 2.7\text{ V}$ $I_{OH} = -1.6\text{ mA}$	$V_{CC} - 0.3$	—	—	V	
“L” level output voltage	V_{OL}	All output pins	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	V_{OL}	All output pins	$V_{CC} = 2.7\text{ V}$ $I_{OL} = 2.0\text{ mA}$	—	—	0.4	V	
Open-drain output leakage current	I_{leak}	P50 to P57, P90, P91*1	—	—	0.1	10	μA	
Input leakage current	I_{IL}	Other than P50 to P57, P90 and P91	$V_{CC} = 5.5\text{ V}$ $V_{SS} < V_i < V_{CC}$	-10	—	10	μA	
Pull-up resistance	R	—	$V_{CC} = 5.0\text{ V}$	25	45	100	$\text{k}\Omega$	
	R	—	$V_{CC} = 3.0\text{ V}$	40	95	200	$\text{k}\Omega$	

(Continued)

MB90670/675 Series

(Continued)

($AV_{CC} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-down resistance	R	—	$V_{CC} = 5.0\text{ V}$	25	50	200	$k\Omega$	
	R	—	$V_{CC} = 3.0\text{ V}$	40	100	400	$k\Omega$	
Power supply current	I_{CC}	—	Internal operation at 16 MHz V_{CC} at 5.0 V	—	50	70	mA	Normal operation*2
	I_{CCS}	—	Internal operation at 16 MHz V_{CC} at 5.0 V	—	10	30	mA	In sleep mode*2
	I_{CC}	—	Internal operation at 8 MHz V_{CC} at 3.0 V	—	12	20	mA	Normal operation*2
	I_{CCS}	—	Internal operation at 8 MHz V_{CC} at 3.0 V	—	2.5	10	mA	In sleep mode*2
	I_{CCH}	—	$T_A = +25^\circ\text{C}$	—	0.1	10	μA	In stop mode and hardware standby mode*2
Input capacitance	C_{IN}	Other than AV_{CC} , AV_{SS} , V_{CC} , V_{SS}	—	—	10	—	pF	

*1: Only MB90675 series has P90 and P91 pins.

*2: The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice.

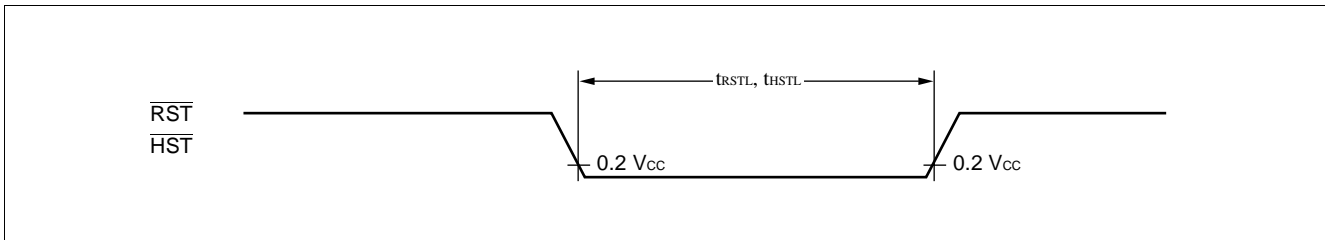
4. AC Characteristics

(1) Reset Input Timing, Hardware Standby Input Timing

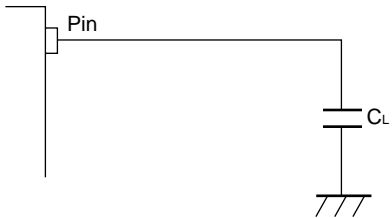
($AV_{CC} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	\overline{RST}	—	16 t_{CP}^*	—	ns	
Hardware standby input time	t_{HSTL}	\overline{HST}	—	16 t_{CP}^*	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timings.”



• Measurement conditions for AC ratings



C_L is a load capacitance connected to a pin under test.

CLK, ALE: $C_L = 30\text{ pF}$

Address data bus (AD15 to AD00), \overline{RD} , \overline{WR} : $C_L = 80\text{ pF}$

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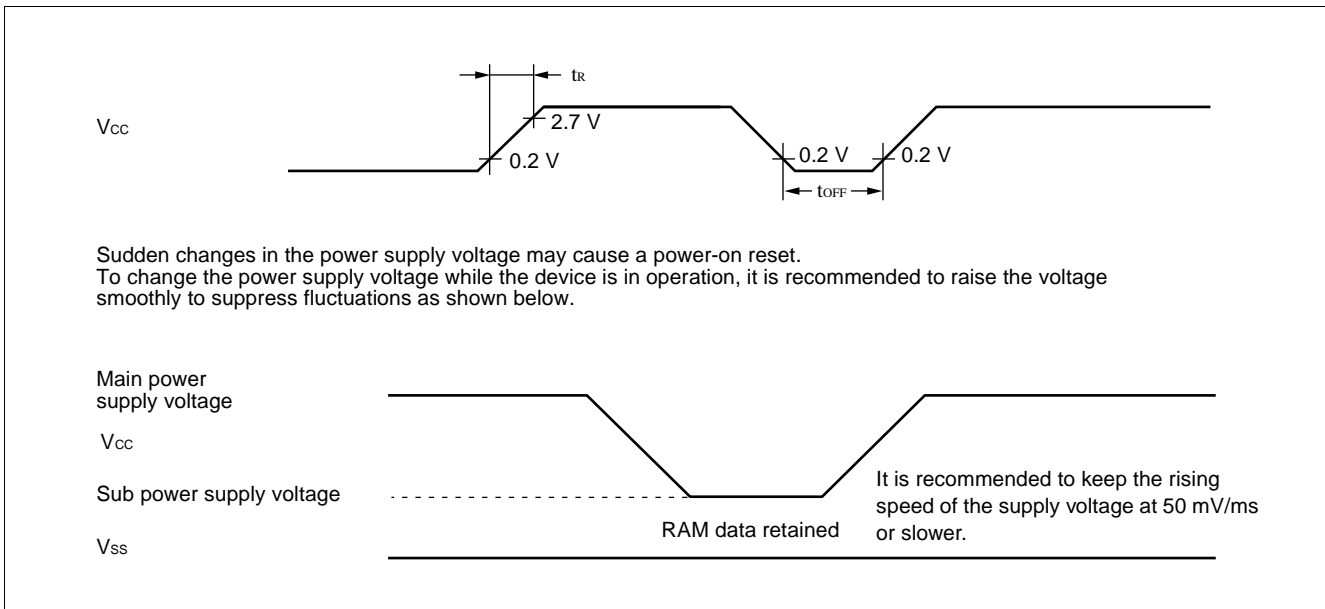
(2) Specification for Power-on Reset

($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	—	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}	—	1	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

- Notes:
- The above ratings are values for causing a power-on reset.
 - When \overline{HST} is set to "L" level, apply power according to this table to cause a power-on reset irrespective of whether or not a power-on reset is required.
 - For built-in resources in the device, re-apply power to the resources to cause a power-on reset.
 - There are internal registers which can be initialized only by a power-on reset. Apply power according to this rating to ensure initialization of the registers.



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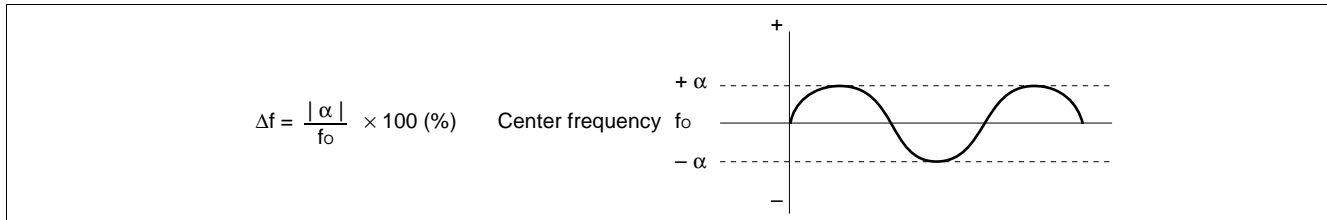
(3) Clock Timing

- Operation at 5.0 V ± 10%

(AV_{SS} = V_{SS} = 0.0 V, T_A = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F _C	X0, X1	—	3	—	32	MHz	
Clock cycle time	t _c	X0, X1		31.25	—	333	ns	
Input clock pulse width	P _{WH} , P _{WL}	X0		10	—	—	ns	Recommended duty ratio of 30% to 70%
Input clock rising/falling time	t _{CR} , t _{CF}	X0		—	—	5	ns	
Internal operating clock frequency	f _{CP}	—		1.5	—	16	MHz	
Internal operating clock cycle time	t _{CP}	—		62.5	—	666	ns	
Frequency fluctuation rate locked	Δf	P37/CLK		—	—	3	%	*

* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.



The PLL frequency deviation changes periodically from the preset frequency “(about CLK × (1CYC to 50 CYC))”, thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

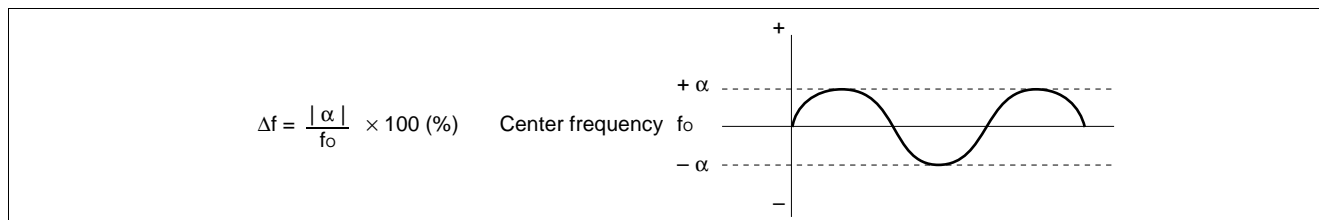
MB90670/675 Series

• Operation at $V_{CC} = 2.7\text{ V}$ (minimum value)

($A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

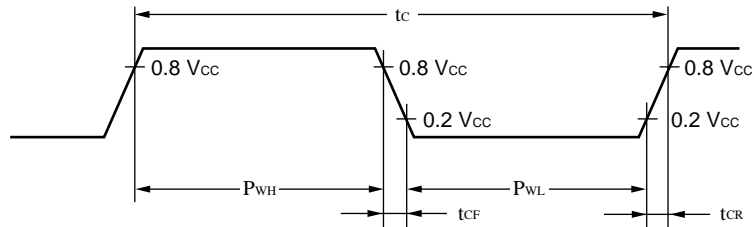
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	—	3	—	16	MHz	
Clock cycle time	t_c	X0, X1		62.5	—	333	ns	
Input clock pulse width	P_{WH}, P_{WL}	X0		20	—	—	ns	Recommended duty ratio of 30% to 70%
Input clock rising/falling time	t_{CR}, t_{CF}	X0		—	—	5	ns	
Internal operating clock frequency	f_{CP}	—		1.5	—	8	MHz	
Internal operating clock cycle time	t_{CP}	—		125	—	666	ns	
Frequency fluctuation rate locked	Δf	P37/CLK		—	—	3	%	*

* : The frequency fluctuation rate is the maximum deviation rate of the preset center frequency when the multiplied PLL signal is locked.

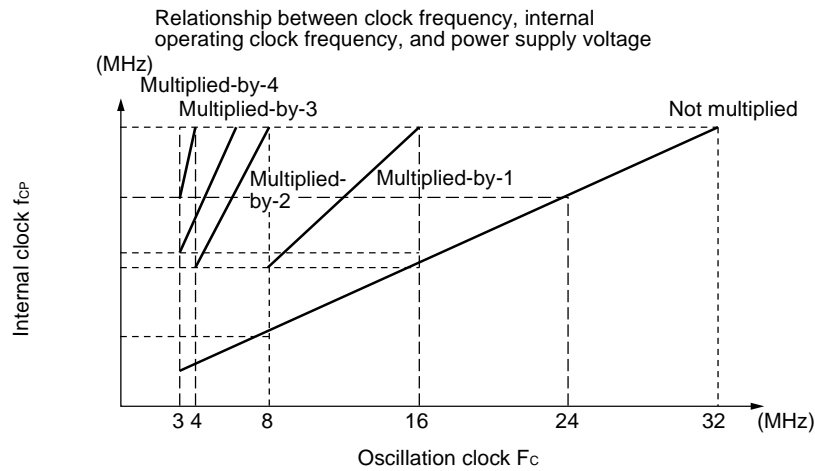
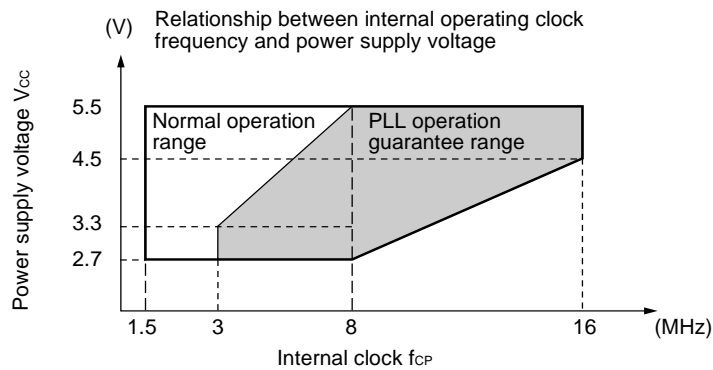


The PLL frequency deviation changes periodically from the preset frequency “(about $CLK \times (1\text{CYC}$ to $50\text{CYC})$ ”, thus minimizing the chance of worst values to be repeated (errors are minimal and negligible for pulses with long intervals).

• Clock timing



• PLL operation guarantee range



Note: The operation guarantee range on the lower voltage is 2.7 V for the evaluation chips.

The AC ratings are measured for the following measurement reference voltages.

• Input signal waveform

Hysteresis input pin



Pins other than hysteresis input/MD input



• Output signal waveform

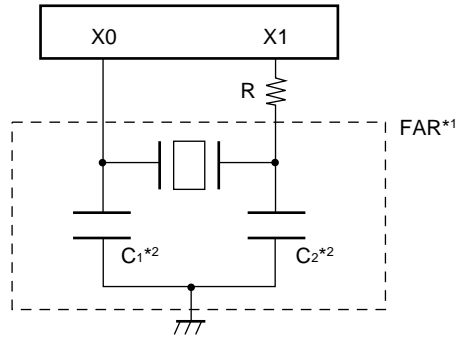
Output pin



MB90670/675 Series

(4) Recommended Resonator Manufacturers

- Sample application of piezoelectric resonator (FAR family)

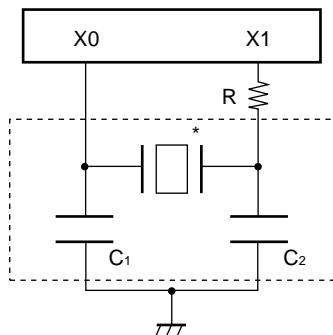


*1: Fujitsu Acoustic Resonator

FAR part number (built-in capacitor type)	Frequency (MHz)	Dumping resistor	Initial deviation of FAR frequency ($T_A = +25^\circ\text{C}$)	Temperature characteristics of FAR frequency ($T_A = -20^\circ\text{C}$ to $+60^\circ\text{C}$)	Loading capacitors*2
FAR-C4□C-2000-□20	2.00	510 Ω	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□A-4000-□01	4.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-4000-□02	4.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-4000-□00	4.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-8000-□02	8.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-12000-□02	12.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-16000-□02	16.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-20000-L14B	20.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□B-24000-L14A	24.00	—	$\pm 0.5\%$	$\pm 0.5\%$	Built-in

Inquiry: FUJITSU LIMITED

• Sample application of ceramic resonator



• Mask ROM product

Resonator manufacturer	Resonator	Frequency (MHz)	C ₁ (pF)	C ₂ (pF)	R
Kyocera Corporation	KBR-2.0MS	2.00	150	150	Not required
	PBRC-2.00A	2.00	150	150	Not required
	KBR-4.0MSA	4.00	33	33	680 Ω
	KBR-4.0MKS	4.00	Built-in	Built-in	680 Ω
	PBRC4.00A	4.00	33	33	680 Ω
	PBRC4.00B	4.00	Built-in	Built-in	680 Ω
	KBR-6.0MSA	6.00	33	33	Not required
	KBR-6.0MKS	6.00	Built-in	Built-in	Not required
	PBRC6.00A	6.00	33	33	Not required
	PBRC6.00B	6.00	Built-in	Built-in	Not required
	KBR-8.0M	8.00	33	33	560 Ω
	PBRC8.00A	8.00	33	33	Not required
	PBRC8.00B	8.00	Built-in	Built-in	Not required
	KBR-10.0M	10.00	33	33	330 Ω
	PBRC10.00B	10.00	Built-in	Built-in	680 Ω
	KBR-12.0M	12.00	33	33	330 Ω
PBRC-12.00B	12.00	Built-in	Built-in	680 Ω	
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CST2.00MG040	2.00	Built-in	Built-in	Not required
	CSA4.00MG040	4.00	100	100	Not required
	CST4.00MGW040	4.00	Built-in	Built-in	Not required
	CSA6.00MG	6.00	30	30	Not required
	CST6.00MGW	6.00	Built-in	Built-in	Not required
	CSA8.00MTZ	8.00	30	30	Not required
	CST8.00MTW	8.00	Built-in	Built-in	Not required

(Continued)

MB90670/675 Series

(Continued)

Resonator manufacturer	Resonator	Frequency (MHz)	C ₁ (pF)	C ₂ (pF)	R
Murata Mfg. Co., Ltd.	CSA10.0MTZ	10.00	30	30	Not required
	CST10.0MTW	10.00	Built-in	Built-in	Not required
	CSA12.0MTZ	12.00	30	30	Not required
	CST12.0MTW	12.00	Built-in	Built-in	Not required
	CSA16.00MXZ040	16.00	15	15	Not required
	CST16.00MXW0C3	16.00	Built-in	Built-in	Not required
	CSA20.00MXZ040	20.00	10	10	Not required
	CSA24.00MXZ040	24.00	5	5	Not required
	CST24.00MXW0H1	24.00	Built-in	Built-in	Not required
	CSA32.00MXZ040	32.00	5	5	Not required
CST32.00MXW040	32.00	Built-in	Built-in	Not required	
TDK Corporation	FCR4.0MC5	4.00	Built-in	Built-in	Not required

• One-time product

Resonator manufacturer	Resonator	Frequency (MHz)	C ₁ (pF)	C ₂ (pF)	R
Murata Mfg. Co., Ltd.	CSTCS4.00MG0C5	4.0	Built-in	Built-in	Not required
	CST8.00MTW	8.00	Built-in	Built-in	Not required
	CSACS8.00MT	8.00	30	30	Not required
	CSA10.0MTZ	10.00	30	30	Not required
	CST10.0MTW	10.00	Built-in	Built-in	Not required
TDK Corporation	FCR4.0MC5	4.00	Built-in	Built-in	Not required

Inquiry: Kyocera Corporation

- AVX Corporation
North American Sales Headquarters: TEL 1-803-448-9411
- AVX Limited
European Sales Headquarters: TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
Asian Sales Headquarters: TEL 852-363-3303

Murata Mfg. Co., Ltd.

- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

TDK Corporation

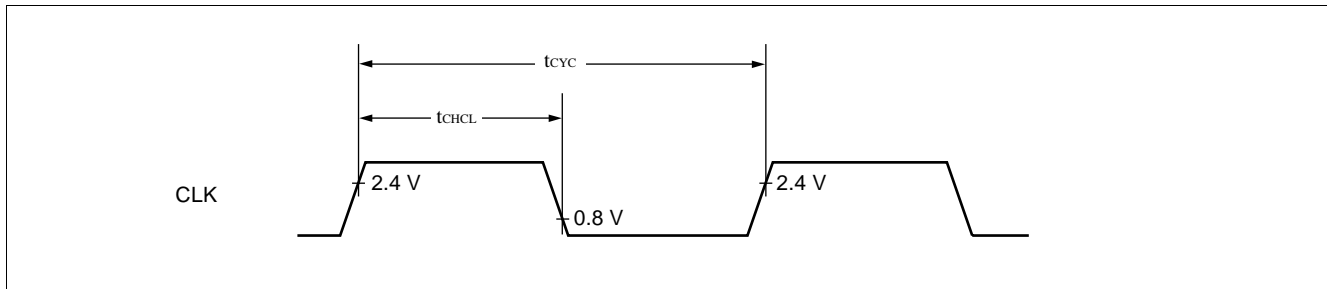
- TDK Corporation of America
Chicago Regional Office: TEL 1-708-803-6100
- TDK Electronics Europe GmbH
Components Division: TEL 49-2102-9450
- TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- TDK Hongkong Co., Ltd.: TEL 852-736-2238
- Korea Branch, TDK Corporation: TEL 82-2-554-6633

(5) Clock Output Timing

($V_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	$1 t_{CP}^*$	—	ns	
CLK $\uparrow \rightarrow$ CLK \downarrow	t_{CHCL}	CLK		$1 t_{CP}^*/2 - 20$	$1 t_{CP}^*/2 + 20$	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timing”.



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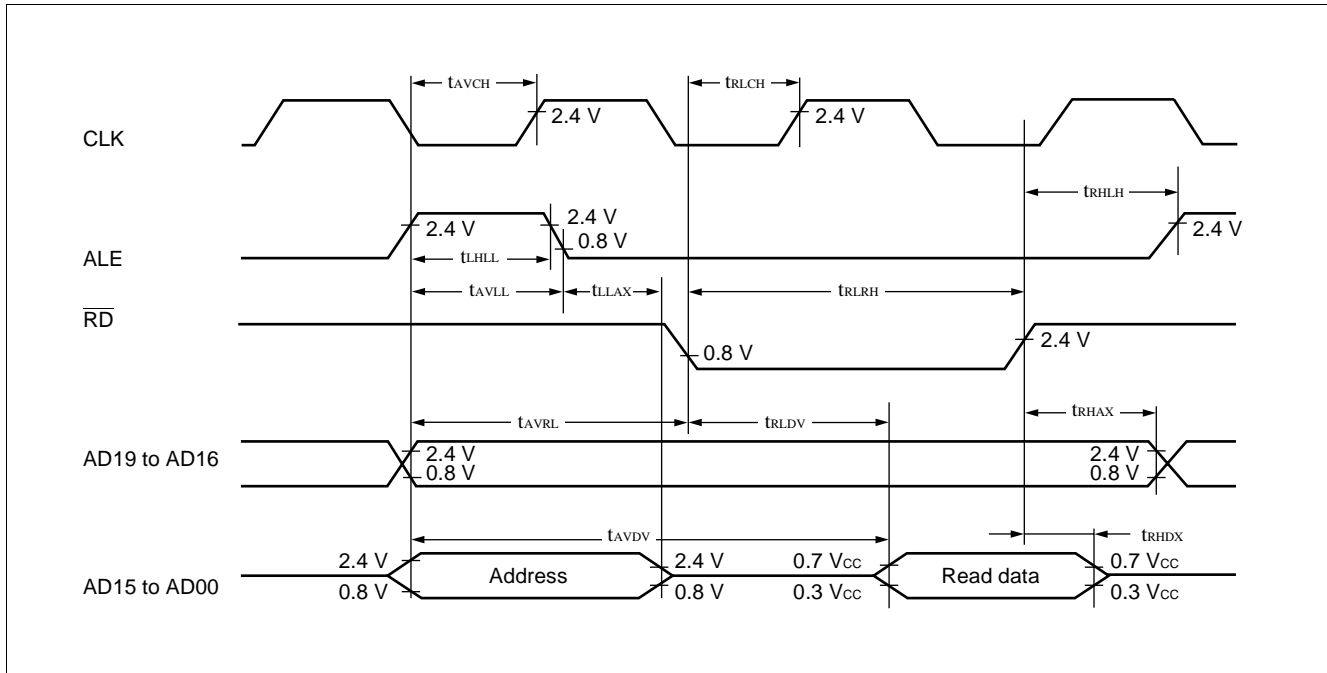
(6) Bus Read Timing

($V_{CC} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t _{LHLL}	ALE	$V_{CC} = 5.0\text{ V} \pm 10\%$	$1\ t_{CP}^*/2 - 20$	—	ns	
	t _{LHLL}	ALE	$V_{CC} = 3.0\text{ V} \pm 10\%$	$1\ t_{CP}^*/2 - 35$	—	ns	
Effective address → ALE ↓ time	t _{AVLL}	AD15 to AD00	$V_{CC} = 5.0\text{ V} \pm 10\%$	$1\ t_{CP}^*/2 - 25$	—	ns	
	t _{AVLL}	AD15 to AD00	$V_{CC} = 3.0\text{ V} \pm 10\%$	$1\ t_{CP}^*/2 - 40$	—	ns	
ALE ↓ → address effective time	t _{LLAX}	AD15 to AD00	—	$1\ t_{CP}^*/2 - 15$	—	ns	
Effective address → $\overline{\text{RD}}$ ↓ time	t _{AVRL}	AD15 to AD00	—	$1\ t_{CP}^* - 15$	—	ns	
Effective address → read data time	t _{AVDV}	AD15 to AD00	$V_{CC} = 5.0\text{ V} \pm 10\%$	—	$5\ t_{CP}^*/2 - 60$	ns	
	t _{AVDV}	AD15 to AD00	$V_{CC} = 3.0\text{ V} \pm 10\%$	—	$5\ t_{CP}^*/2 - 80$	ns	
$\overline{\text{RD}}$ pulse width	t _{RLRH}	$\overline{\text{RD}}$	—	$3\ t_{CP}^*/2 - 20$	—	ns	
$\overline{\text{RD}}$ ↓ → read data time	t _{RLDV}	AD15 to AD00	$V_{CC} = 5.0\text{ V} \pm 10\%$	—	$3\ t_{CP}^*/2 - 60$	ns	
	t _{RLDV}	AD15 to AD00	$V_{CC} = 3.0\text{ V} \pm 10\%$	—	$3\ t_{CP}^*/2 - 80$	ns	
$\overline{\text{RD}}$ ↑ → data hold time	t _{RHDX}	AD15 to AD00	—	0	—	ns	
$\overline{\text{RD}}$ ↑ → ALE ↑ time	t _{RHLH}	$\overline{\text{RD}}$, ALE	—	$1\ t_{CP}^*/2 - 15$	—	ns	
$\overline{\text{RD}}$ ↑ → address disappear time	t _{RHAX}	$\overline{\text{RD}}$, A19 to A16	—	$1\ t_{CP}^*/2 - 10$	—	ns	
Effective address → CLK ↑ time	t _{AVCH}	CLK, A19 to A16	—	$1\ t_{CP}^*/2 - 20$	—	ns	
$\overline{\text{RD}}$ ↓ → CLK ↑ time	t _{RLCH}	$\overline{\text{RD}}$, CLK	—	$1\ t_{CP}^*/2 - 20$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timing”.

MB90670/675 Series



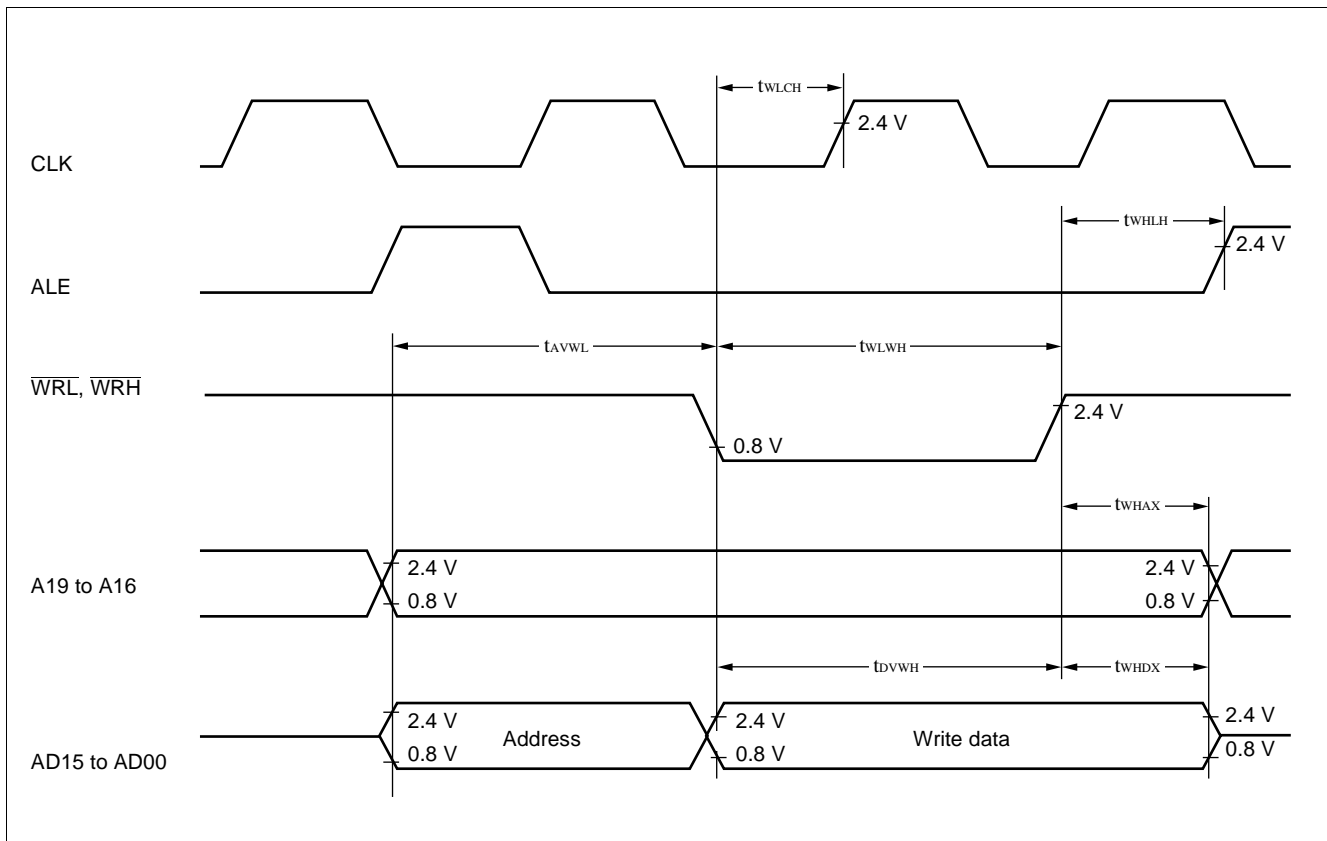
MB90670/675 Series

(7) Bus Write Timing

($V_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Effective address $\rightarrow \overline{WR}$ \downarrow time	t_{AVWL}	A19 to A00	—	$1 t_{CP} - 15$	—	ns	
\overline{WR} pulse width	t_{WLWH}	\overline{WR}		$3 t_{CP}^*/2 - 20$	—	ns	
Write data $\rightarrow \overline{WR}$ \uparrow time	t_{DVWH}	AD15 to AD00		$3 t_{CP}^*/2 - 20$	—	ns	
\overline{WR} \uparrow \rightarrow data hold time	t_{WHDX}	AD15 to AD00	$V_{CC} = 5.0\text{ V} \pm 10\%$	20	—	ns	
	t_{WHDX}	AD15 to AD00	$V_{CC} = 3.0\text{ V} \pm 10\%$	30	—	ns	
\overline{WR} \uparrow \rightarrow address disappear time	t_{WHAX}	A19 to A00	—	$1 t_{CP}^*/2 - 10$	—	ns	
\overline{WR} \uparrow \rightarrow ALE \uparrow time	t_{WHLH}	\overline{WRL} , ALE		$1 t_{CP}^*/2 - 15$	—	ns	
\overline{WR} \downarrow \rightarrow CLK \uparrow time	t_{WLCH}	\overline{WRH} , CLK		$1 t_{CP}^*/2 - 20$	—	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timing”.

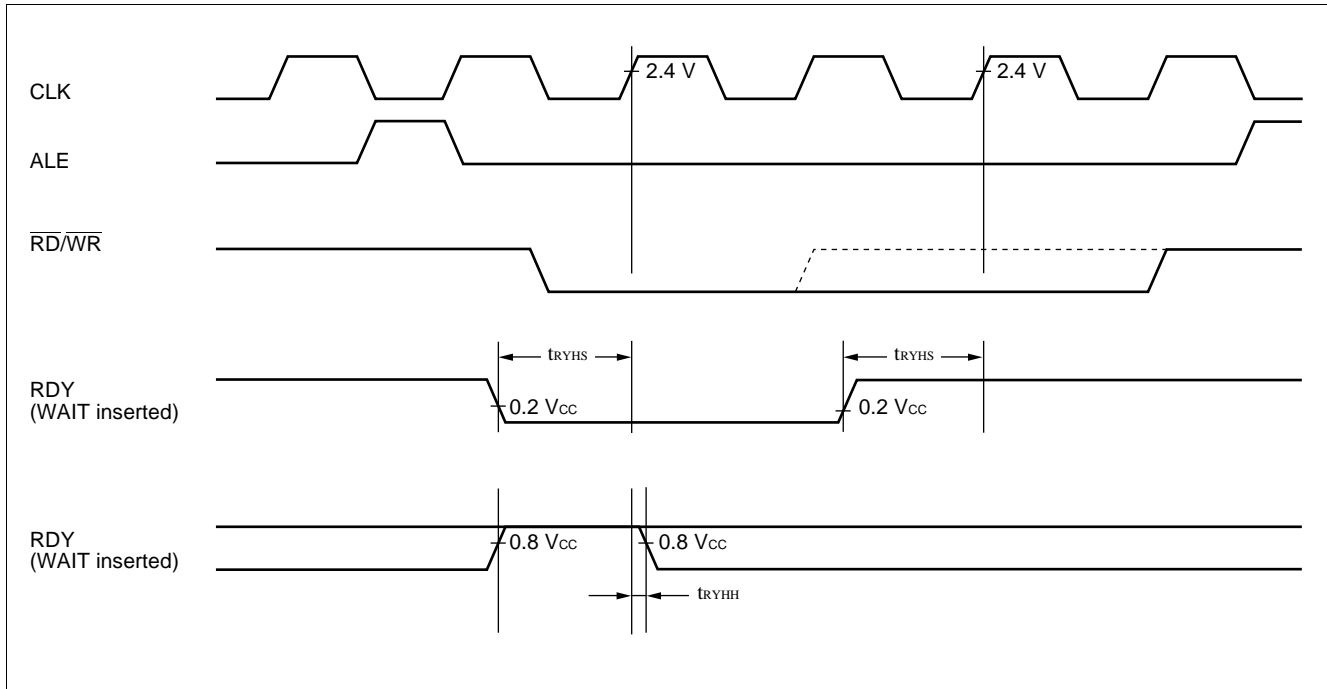


(8) Ready Input Timing

($A_{V_{CC}} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	$V_{CC} = 5.0\text{ V} \pm 10\%$	45	—	ns	
	t_{RYHS}	RDY	$V_{CC} = 3.0\text{ V} \pm 10\%$	70	—	ns	
RDY hold time	t_{RYHH}	RDY	—	0	—	ns	

Note: Use the auto-ready function when the setup time for the rising of the RDY signal is not sufficient.



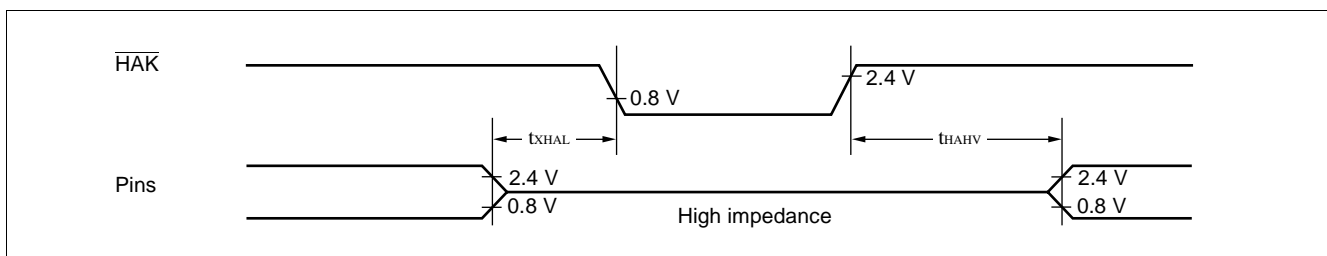
(9) Hold Timing

($A_{V_{CC}} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pins in floating status → $\overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	$1 t_{CP}^*$	ns	
$\overline{\text{HAK}} \uparrow$ → pin valid time	t_{HAHV}	$\overline{\text{HAK}}$	—	$1 t_{CP}^*$	$2 t_{CP}^*$	ns	

* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timing”.

Note: More than 1 machine cycle is needed before $\overline{\text{HAK}}$ changes after HRQ pin is fetched.



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(10) UART0 Timing

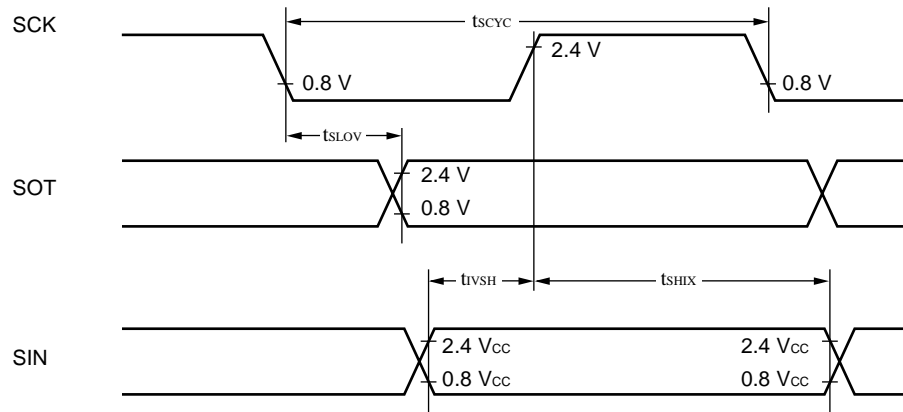
($A_{V_{CC}} = V_{CC} = 5.0\text{ V} \pm 10\%$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t _{SCYC}	—	—	8 t _{CP} *	—	ns	Internal shift clock mode C _L = 80 pF + 1 TTL for an output pin
SCK ↓ → SOT delay time	t _{SLOV}	—	V _{CC} = 5.0 V ±10%	- 80	80	ns	
	t _{SLOV}	—	V _{CC} = 3.0 V ±10%	- 120	120	ns	
Valid SIN → SCK ↑	t _{IVSH}	—	V _{CC} = 5.0 V ±10%	100	—	ns	
	t _{IVSH}	—	V _{CC} = 3.0 V ±10%	200	—	ns	
SCK ↑ → valid SIN hold time	t _{SHIX}	—	—	1 t _{CP} *	—	ns	External shift clock mode C _L = 80 pF + 1 TTL for an output pin
Serial clock "H" pulse width	t _{SHSL}	—	—	4 t _{CP} *	—	ns	
Serial clock "L" pulse width	t _{SLSH}	—	—	4 t _{CP} *	—	ns	
SCK ↓ → SOT delay time	t _{SLOV}	—	V _{CC} = 5.0 V ±10%	—	150	ns	
	t _{SLOV}	—	V _{CC} = 3.0 V ±10%	—	200	ns	
Valid SIN → SCK ↑	t _{IVSH}	—	V _{CC} = 5.0 V ±10%	60	—	ns	
	t _{IVSH}	—	V _{CC} = 3.0 V ±10%	120	—	ns	
SCK ↑ → valid SIN hold time	t _{SHIX}	—	V _{CC} = 5.0 V ±10%	60	—	ns	
	t _{SHIX}	—	V _{CC} = 3.0 V ±10%	120	—	ns	

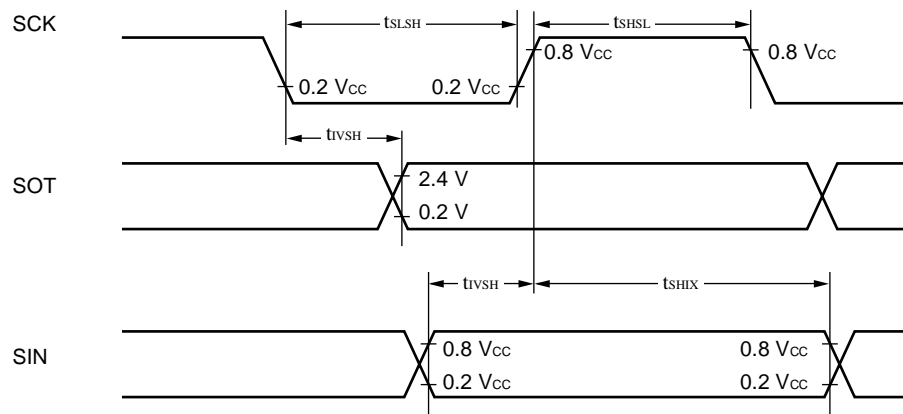
* : For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timing".

- Notes:
- These are AC ratings in the CLK synchronous mode.
 - C_L is the load capacitor connected to pins while testing.

- Internal shift clock mode



- External shift clock mode



MB90670/675 Series

(11) UART1 Timing

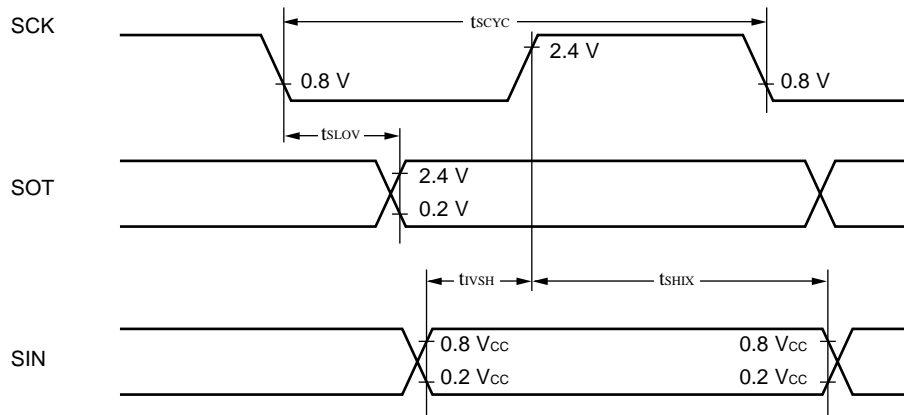
($A_{V_{CC}} = V_{CC} = 5.0\text{ V} \pm 10\%$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	tSCYC	—	—	8 t _{CP} *	—	ns	Internal shift clock mode C _L = 80 pF + 1 TTL for an output pin
SCK ↓ → SOT delay time	tSLOV	—	V _{CC} = 5.0 V ±10%	- 80	80	ns	
	tSLOV	—	V _{CC} = 3.0 V ±10%	- 120	120	ns	
Valid SIN → SCK ↑	tIVSH	—	V _{CC} = 5.0 V ±10%	100	—	ns	
	tIVSH	—	V _{CC} = 3.0 V ±10%	200	—	ns	
SCK ↑ → valid SIN hold time	tSHIX	—	—	1 t _{CP} *	—	ns	External shift clock mode C _L = 80 pF + 1 TTL for an output pin
Serial clock "H" pulse width	tSHSL	—		4 t _{CP} *	—	ns	
Serial clock "L" pulse width	tSLSH	—		4 t _{CP} *	—	ns	
SCK ↓ → SOT delay time	tSLOV	—	V _{CC} = 5.0 V ±10%	—	150	ns	
	tSLOV	—	V _{CC} = 3.0 V ±10%	—	200	ns	
Valid SIN → SCK ↑	tIVSH	—	V _{CC} = 5.0 V ±10%	60	—	ns	
	tIVSH	—	V _{CC} = 3.0 V ±10%	120	—	ns	
SCK ↑ → valid SIN hold time	tSHIX	—	V _{CC} = 5.0 V ±10%	60	—	ns	
	tSHIX	—	V _{CC} = 3.0 V ±10%	120	—	ns	

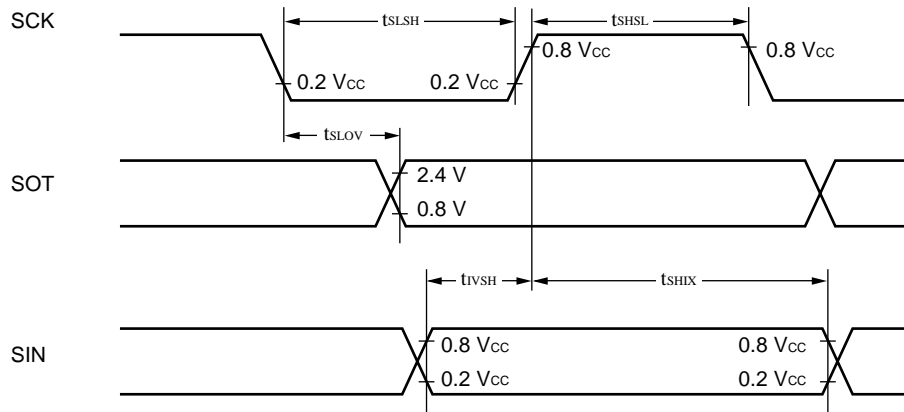
* : For t_{CP} (internal operating clock cycle time), refer to "(3) Clock Timing".

- Notes:
- These are AC ratings in the CLK synchronous mode.
 - C_L is the load capacitor connected to pins while testing.

- Internal shift clock mode



- External shift clock mode



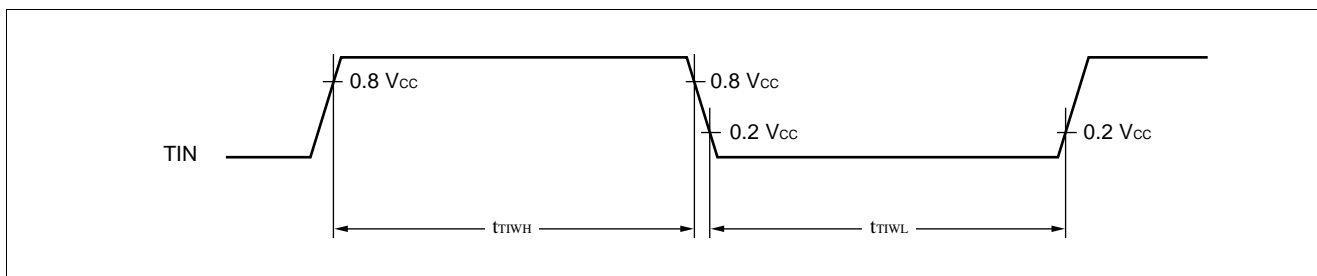
MB90670/675 Series

(12) Timer Input Timing

($A_{V_{CC}} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} , t_{TIWL}	TIN0, TON1	—	$4 t_{CP}^*$	—	ns	

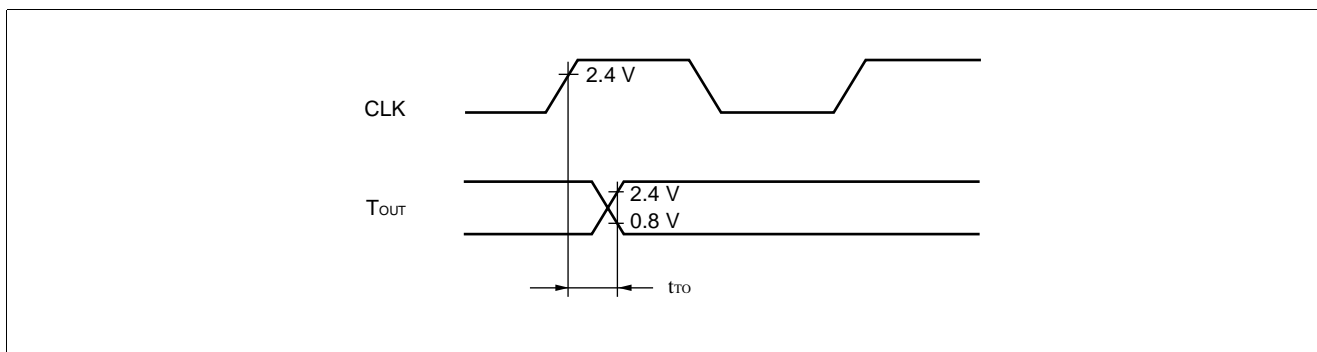
* : For t_{CP} (internal operating clock cycle time), refer to “(3) Clock Timing”.



(13) Timer Output Timing

($A_{V_{CC}} = V_{CC} = 2.7 \text{ V}$ to 5.5 V , $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK \uparrow \rightarrow T_{OUT} transition time	t_{TO}	TOT0, TOT1	$V_{CC} = 5.0 \text{ V} \pm 10\%$	30	—	ns	
	t_{TO}	TOT0, TOT1	$V_{CC} = 3.0 \text{ V} \pm 10\%$	80	—	ns	

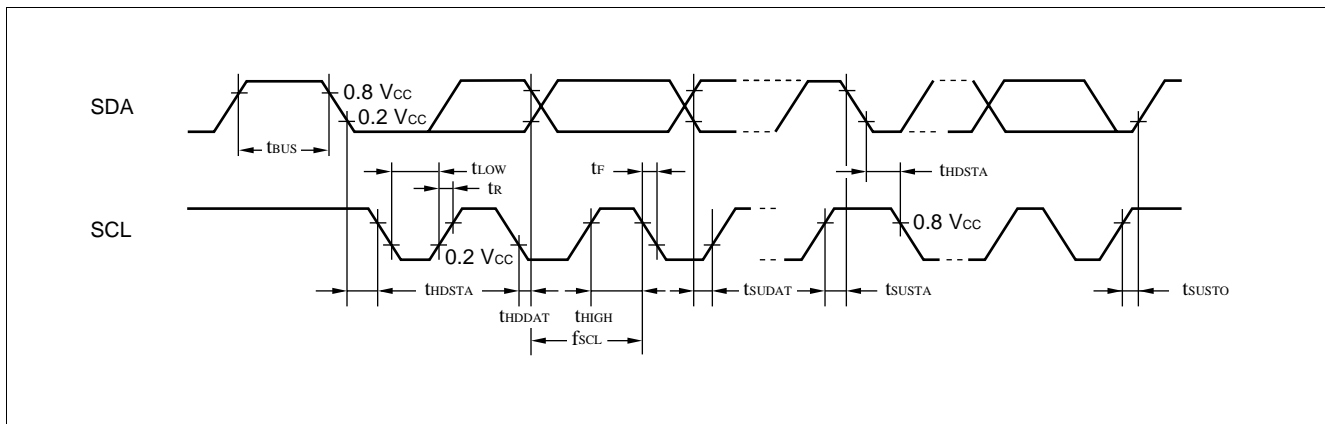


(14) I²C Timing

($V_{CC} = V_{SS} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
SCL clock frequency	f_{SCL}	—	—	0	100	kHz	
Bus free time between stop and start conditions	t_{BUS}	—		4.7	—	μs	
Hold time (re-transmission) start	t_{HDSTA}	—		4.0	—	μs	The first clock pulse is generated after this period.
LOW status hold time of SCL clock	t_{LOW}	—		4.7	—	μs	
HIGH status hold time of SCL clock	t_{HIGH}	—		4.0	—	μs	
Setup time for conditions for starting re-transmission	t_{SUSTA}	—		4.7	—	μs	
Data hold time	t_{HDDAT}	—		0	—	μs	
Data setup time	t_{SUDAT}	—		250	—	ns	
Rising time of SDA and SCL signals	t_R	—		—	1000	ns	
Falling time of SDA and SCL signals	t_F	—		—	300	ns	
Setup time for stop conditions	t_{SUSTO}	—		4.0	—	μs	

Note: Only MB90675 series has I²C.



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5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = 2.7\text{ V to }5.5\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $2.7\text{ V} \leq AV_{RH} - AV_{RL}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution	—	—	—	—	—	10	bit
Total error	—	—		—	—	± 3.0	LSB
Linearity error	—	—		—	—	± 2.0	LSB
Differential linearity error	—	—		—	—	± 1.5	LSB
Zero transition voltage	V_{OT}	AN0 to AN7		—	AVRL - 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB
Full-scale transition voltage	V_{FST}	AN0 to AN7	—	AVRH - 4.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	mV
Conversion time	—	—	$V_{CC} = 5.0\text{ V} \pm 10\%$ at machine clock of 16 MHz	6.125	—	—	μs
	—	—	$V_{CC} = 3.0\text{ V} \pm 10\%$ at machine clock of 8 MHz	12.25	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN7	—	—	0.1	10	μA
Analog input voltage	V_{AIN}	AN0 to AN7		AVRL	—	AVRH	V
Reference voltage	—	AVRH		AVRL - 2.7	—	AV_{CC}	V
	—	AVRL		0	—	AVRH - 2.7	V
Power supply current	I_A	AV_{CC}		—	—	3	—
	I_{AH}	AV_{CC}	Supply current when CPU stopped and A/D converter not in operation ($V_{CC} = AV_{CC} =$ $AVRH = 5.0\text{ V}$)	—	—	5	μA
Reference voltage supply current	I_R	AVRH	—	—	200	—	μA
	I_{RH}	AVRH	Supply current when CPU stopped and A/D converter not in operation ($V_{CC} = AV_{CC} =$ $AVRH = 5.0\text{ V}$)	—	—	5	μA
Offset between channels	—	AN0 to AN7	—	—	—	4	LSB

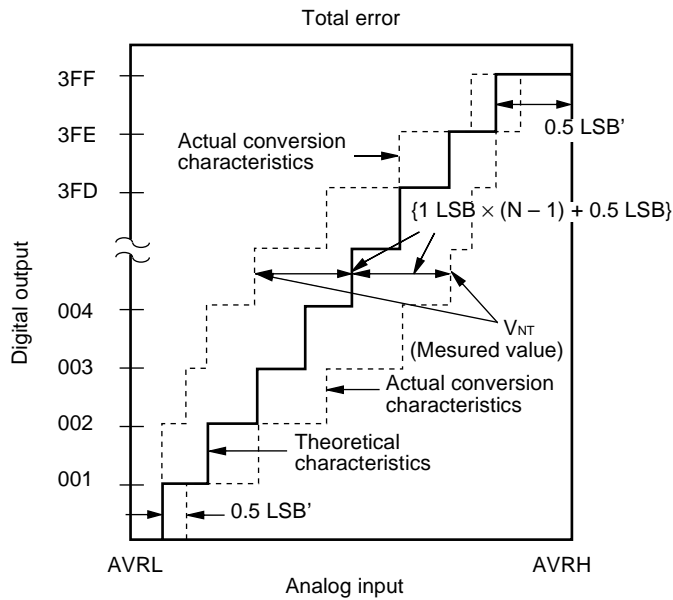
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB}' = (\text{Theoretical value}) \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'} \text{ [LSB]}$$

$$V_{0T}' (\text{Theoretical value}) = \text{AVRL} + 0.5 \text{ LSB}' \text{ [V]}$$

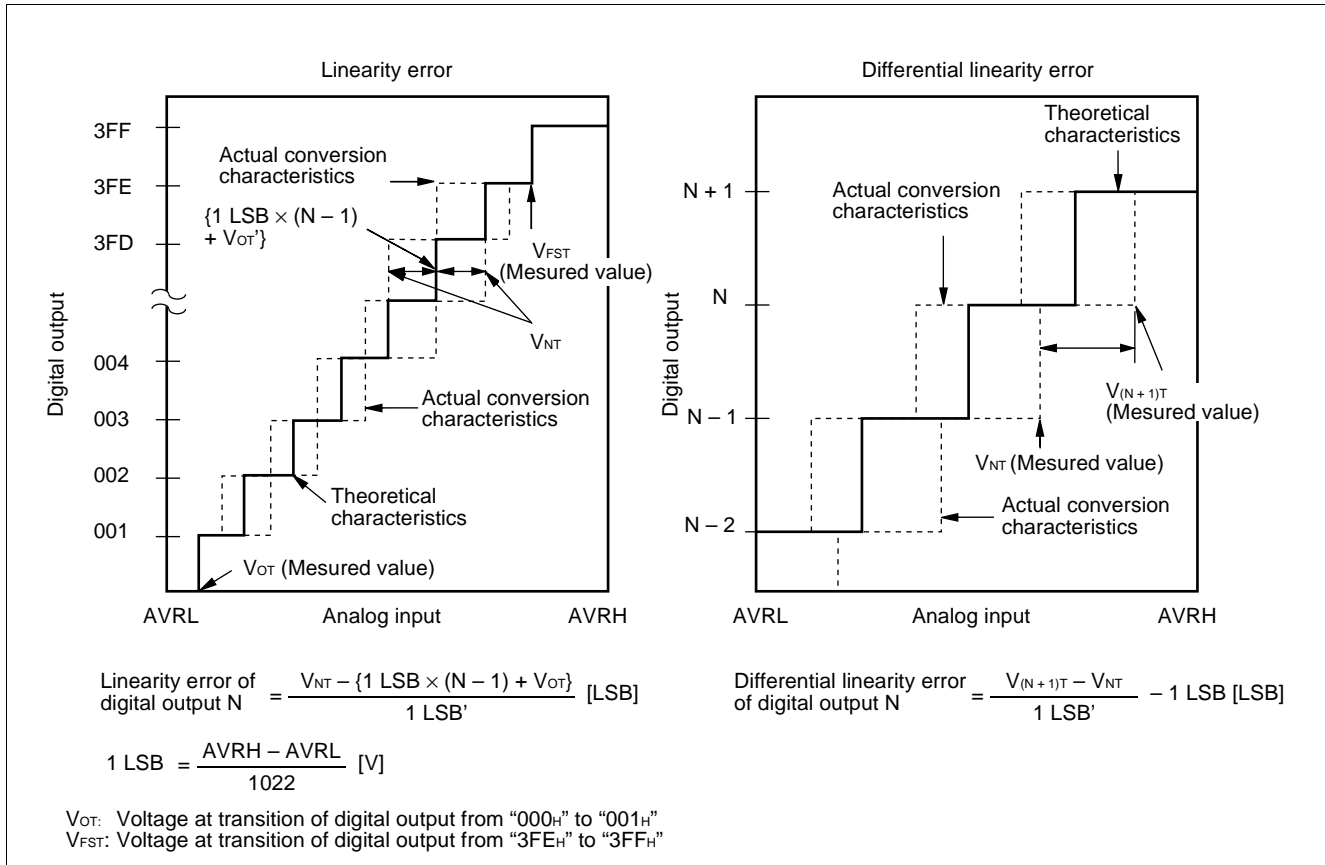
V_{NT} : Voltage at a transition of digital output from $(N - 1)$ to N

$$V_{FST}' (\text{Theoretical value}) = \text{AVRH} - 1.5 \text{ LSB}' \text{ [V]}$$

(Continued)

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(Continued)



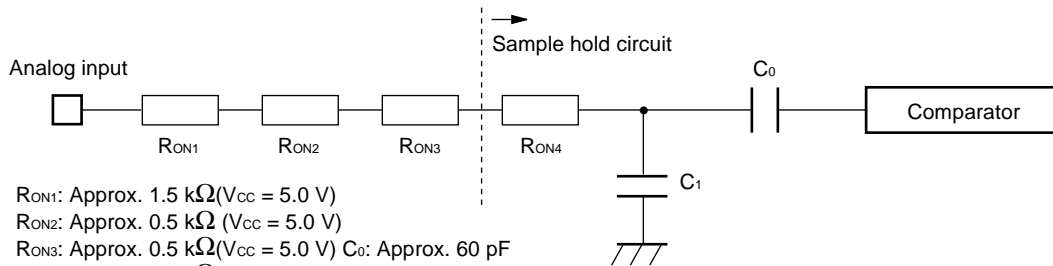
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions. Output impedance values of the external circuit of 7 kΩ or lower are recommended.

When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling time for analog voltages may not be sufficient (sampling time = 3.75 μs @ machine clock of 16 MHz).

• Block diagram of analog input circuit model



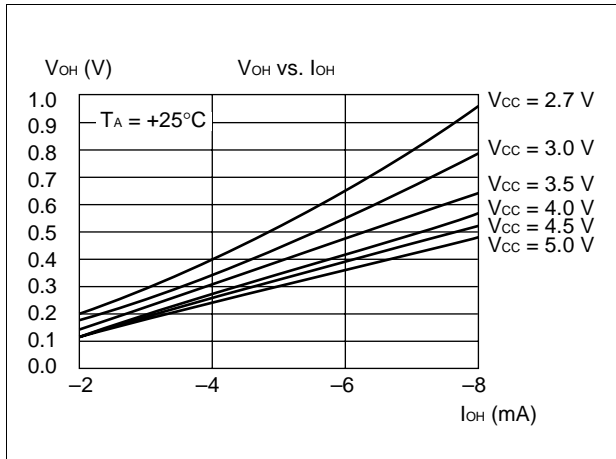
Note: Listed values must be considered as standards.

• Error

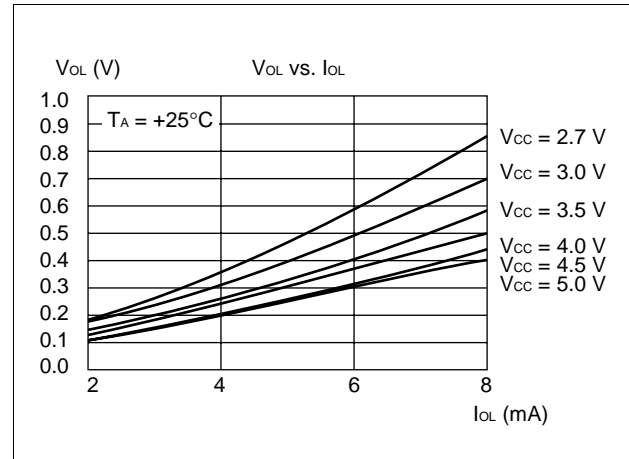
The smaller the $|AVRH - AVRL|$, the greater the error would become relatively.

EXAMPLE CHARACTERISTICS

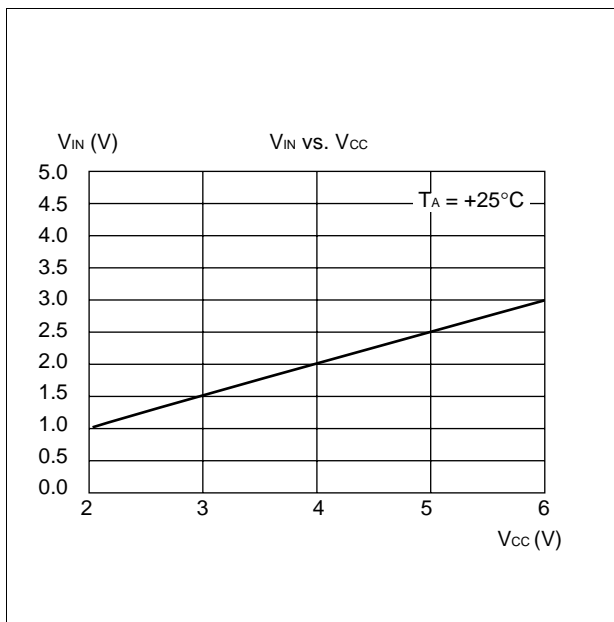
(1) "H" Level Output Voltage



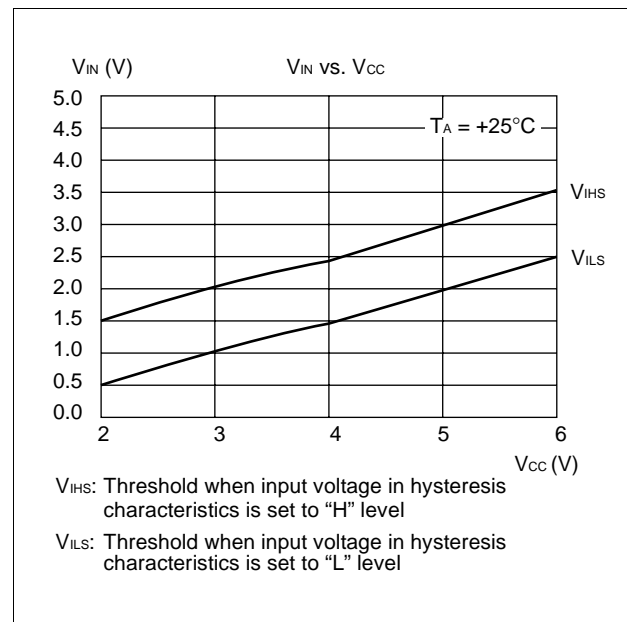
(2) "L" Level Output Voltage



(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)

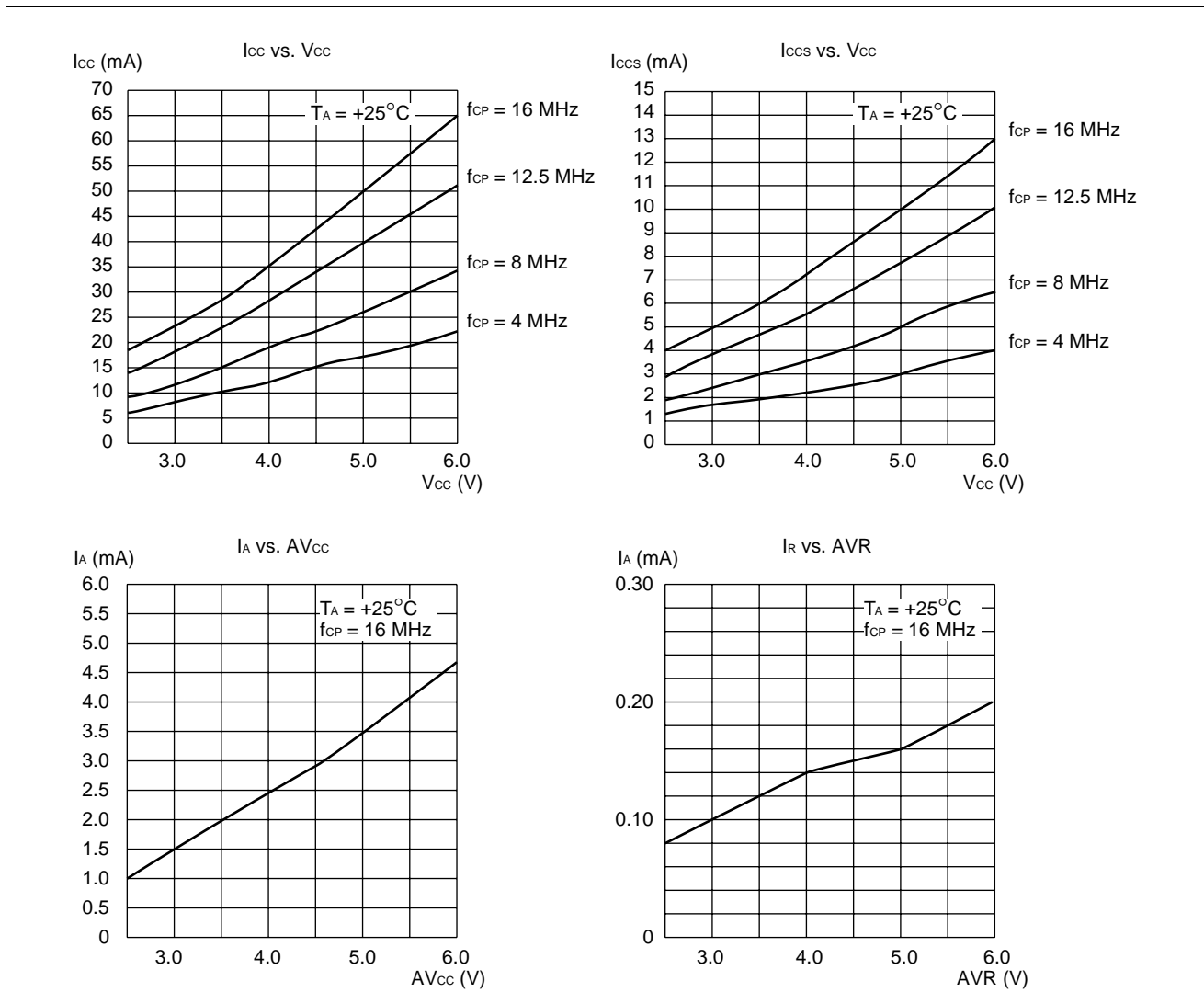


(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

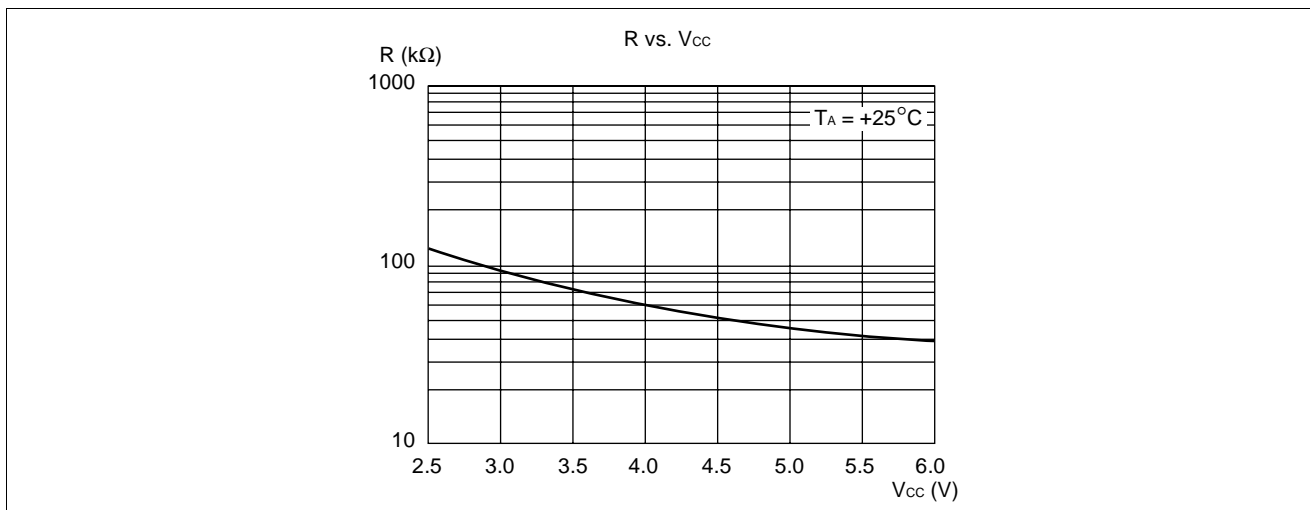


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(5) Power Supply Current (f_{CP} = Internal Operating Clock Frequency)



(6) Pull-up Resistance



■ INSTRUCTIONS (340 INSTRUCTIONS)

Table 1 Explanation of Items in Tables of Instructions

Item	Meaning
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler. Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction.
#	Indicates the number of bytes.
~	Indicates the number of cycles. m : When branching n : When not branching See Table 4 for details about meanings of other letters in items.
RG	Indicates the number of accesses to the register during execution of the instruction. It is used calculate a correction value for intermittent operation of CPU.
B	Indicates the correction value for calculating the number of actual cycles during execution of the instruction. (Table 5) The number of actual cycles during execution of the instruction is the correction value summed with the value in the “~” column.
Operation	Indicates the operation of instruction.
LH	Indicates special operations involving the upper 8 bits of the lower 16 bits of the accumulator. Z : Transfers “0”. X : Extends with a sign before transferring. – : Transfers nothing.
AH	Indicates special operations involving the upper 16 bits in the accumulator. * : Transfers from AL to AH. – : No transfer. Z : Transfers 00 _H to AH. X : Transfers 00 _H or FF _H to AH by signing and extending AL.
I	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). * : Changes due to execution of instruction. – : No change. S : Set by execution of instruction. R : Reset by execution of instruction.
S	
T	
N	
Z	
V	
C	
RMW	Indicates whether the instruction is a read-modify-write instruction. (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.) * : Instruction is a read-modify-write instruction. – : Instruction is not a read-modify-write instruction. Note: A read-modify-write instruction cannot be used on addresses that have different meanings depending on whether they are read or written.

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Table 2 Explanation of Symbols in Tables of Instructions

Symbol	Meaning
A	32-bit accumulator The bit length varies according to the instruction. Byte : Lower 8 bits of AL Word : 16 bits of AL Long : 32 bits of AL:AH
AH AL	Upper 16 bits of A Lower 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Compact direct addressing
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Direct addressing Physical direct addressing Bit 0 to bit 15 of addr24 Bit 16 to bit 23 of addr24
io	I/O area (000000H to 0000FFH)
imm4 imm8 imm16 imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
()b	Bit address

(Continued)

(Continued)

Symbol	Meaning
rel	Branch specification relative to PC
ear eam	Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

Table 3 Effective Address Fields

Code	Notation	Address format	Number of bytes in address extension *
00 01 02 03 04 05 06 07	R0 R1 R2 R3 R4 R5 R6 R7 RW0 RW1 RW2 RW3 RW4 RW5 RW6 RW7 RL0 (RL0) RL1 (RL1) RL2 (RL2) RL3 (RL3)	Register direct “ea” corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3	Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +	Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8	Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16	Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note: The number of bytes in the address extension is indicated by the “+” symbol in the “#” (number of bytes) column in the tables of instructions.

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Table 4 Number of Execution Cycles for Each Type of Addressing

Code	Operand	(a)	Number of register accesses for each type of addressing
		Number of execution cycles for each type of addressing	
00 to 07	Ri RWi RLi	Listed in tables of instructions	Listed in tables of instructions
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C	@RW0 + RW7	4	2
1D	@RW1 + RW7	4	2
1E	@PC + disp16	2	0
1F	addr16	1	0

Note: “(a)” is used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b) byte		(c) word		(d) long	
	Number of cycles	Number of access	Number of cycles	Number of access	Number of cycles	Number of access
Internal register	+0	1	+0	1	+0	2
Internal memory even address	+0	1	+0	1	+0	2
Internal memory odd address	+0	1	+2	2	+4	4
Even address on external data bus (16 bits)	+1	1	+1	1	+2	2
Odd address on external data bus (16 bits)	+1	1	+4	2	+8	4
External data bus (8 bits)	+1	1	+4	2	+8	4

Notes: • “(b)”, “(c)”, and “(d)” are used in the “~” (number of states) column and column B (correction value) in the tables of instructions.

- When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

Table 6 Correction Values for Number of Cycles Used to Calculate Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus (16 bits)	—	+3
External data bus (8 bits)	+3	—

Notes: • When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

- Because instruction execution is not slowed down by all program fetches in actuality, these correction values should be used for “worst case” calculations.

Table 7 Transfer Instructions (Byte) [41 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
MOV A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	—	—	—	*	*	—	—	—
MOV A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	—	—	—	*	*	—	—	—
MOV A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	—	—	—	*	*	—	—	—
MOV A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	—	—	—	*	*	—	—	—
MOV A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	Z	*	—	—	—	*	*	—	—	—
MOV A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	—	—	—	*	*	—	—	—
MOV A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	—	—	—	*	*	—	—	—
MOV A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	—	—	—	—	*	*	—	—	—
MOV A, @RLi+disp8	3	10	2	(b)	byte (A) ←	Z	*	—	—	—	*	*	—	—	—
MOVN A, #imm4	1	1	0	0	((RLi)+disp8) byte (A) ← imm4	Z	*	—	—	—	R	*	—	—	—
MOVX A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	—	—	—	*	*	—	—	—
MOVX A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	—	—	—	*	*	—	—	—
MOVX A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	—	—	—	*	*	—	—	—
MOVX A, ear	2	2	1	0	byte (A) ← (ear)	X	*	—	—	—	*	*	—	—	—
MOVX A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	X	*	—	—	—	*	*	—	—	—
MOVX A, io	2	3	0	(b)	byte (A) ← (io)	X	*	—	—	—	*	*	—	—	—
MOVX A, #imm8	2	2	0	0	byte (A) ← (io)	X	*	—	—	—	*	*	—	—	—
MOVX A, @A	2	3	0	(b)	byte (A) ← imm8	X	—	—	—	—	*	*	—	—	—
MOVX A, @RWi+disp8	2	5	1	(b)	byte (A) ← ((A))	X	*	—	—	—	*	*	—	—	—
MOVX A, @RLi+disp8	3	10	2	(b)	byte (A) ←	X	*	—	—	—	*	*	—	—	—
					((RWi)+disp8)										
MOV dir, A	2	3	0	(b)	byte (A) ←	—	—	—	—	—	*	*	—	—	—
MOV addr16, A	3	4	0	(b)	((RLi)+disp8)	—	—	—	—	—	*	*	—	—	—
MOV Ri, A	1	2	1	0		—	—	—	—	—	*	*	—	—	—
MOV ear, A	2	2	1	0	byte (dir) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV eam, A	2+	3+ (a)	0	(b)	byte (addr16) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV io, A	2	3	0	(b)	byte (Ri) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV @RLi+disp8, A	3	10	2	(b)	byte (ear) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV Ri, ear	2	3	2	0	byte (eam) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV Ri, eam	2+	4+ (a)	1	(b)	byte (io) ← (A)	—	—	—	—	—	*	*	—	—	—
MOV ear, Ri	2	4	2	0	byte ((RLi) + disp8) ←	—	—	—	—	—	*	*	—	—	—
MOV eam, Ri	2+	5+ (a)	1	(b)	(A)	—	—	—	—	—	*	*	—	—	—
MOV Ri, #imm8	2	2	1	0	byte (Ri) ← (ear)	—	—	—	—	—	*	*	—	—	—
MOV io, #imm8	3	5	0	(b)	byte (Ri) ← (eam)	—	—	—	—	—	—	—	—	—	—
MOV dir, #imm8	3	5	0	(b)	byte (ear) ← (Ri)	—	—	—	—	—	—	—	—	—	—
MOV ear, #imm8	3	2	1	0	byte (eam) ← (Ri)	—	—	—	—	—	*	*	—	—	—
MOV eam, #imm8	3+	4+ (a)	0	(b)	byte (Ri) ← imm8	—	—	—	—	—	—	—	—	—	—
MOV @AL, AH	2	3	0	(b)	byte (io) ← imm8	—	—	—	—	—	*	*	—	—	—
/MOV @A, T					byte (dir) ← imm8 byte (ear) ← imm8										
XCH A, ear	2	4	2	0	byte (eam) ← imm8	Z	—	—	—	—	—	—	—	—	—
XCH A, eam	2+	5+ (a)	0	2× (b)	byte ((A)) ← (AH)	Z	—	—	—	—	—	—	—	—	—
XCH Ri, ear	2	7	4	0		—	—	—	—	—	—	—	—	—	—
XCH Ri, eam	2+	9+ (a)	2	2× (b)		—	—	—	—	—	—	—	—	—	—
					byte (A) ↔ (ear) byte (A) ↔ (eam) byte (Ri) ↔ (ear) byte (Ri) ↔ (eam)										

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 8 Transfer Instructions (Word/Long Word) [38 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	—	*	—	—	—	*	*	—	—	—
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	—	*	—	—	—	*	*	—	—	—
MOVW A, SP	1	1	0	0	word (A) ← (SP)	—	*	—	—	—	*	*	—	—	—
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	—	*	—	—	—	*	*	—	—	—
MOVW A, ear	2	2	1	0	word (A) ← (ear)	—	*	—	—	—	*	*	—	—	—
MOVW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	—	*	—	—	—	*	*	—	—	—
MOVW A, io	2	3	0	(c)	word (A) ← (io)	—	*	—	—	—	*	*	—	—	—
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	—	—	—	—	—	*	*	—	—	—
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	—	*	—	—	—	*	*	—	—	—
MOVW A, @RWi+disp8	2	5	1	(c)	word (A) ← ((RWi)	—	*	—	—	—	*	*	—	—	—
MOVW A, @RLi+disp8	3	10	2	(c)	+disp8)	—	*	—	—	—	*	*	—	—	—
					word (A) ← ((RLi)										
					+disp8)						*	*	—	—	—
MOVW dir, A	2	3	0	(c)		—	—	—	—	—	*	*	—	—	—
MOVW addr16, A	3	4	0	(c)		—	—	—	—	—	*	*	—	—	—
MOVW SP, A	1	1	0	0	word (dir) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, A	1	2	1	0	word (addr16) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW ear, A	2	2	1	0	word (SP) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW eam, A	2+	3+ (a)	0	(c)	word (RWi) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW io, A	2	3	0	(c)	word (ear) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW @RWi+disp8, A	2	5	1	(c)	word (eam) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW @RLi+disp8, A	3	10	2	(c)	word (io) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, ear	2	3	2	(0)	word ((RWi) +disp8) ←	—	—	—	—	—	*	*	—	—	—
MOVW RWi, eam	2+	4+ (a)	1	(c)	(A)	—	—	—	—	—	*	*	—	—	—
MOVW ear, RWi	2	4	2	0	word ((RLi) +disp8) ←	—	—	—	—	—	*	*	—	—	—
MOVW eam, RWi	2+	5+ (a)	1	(c)	(A)	—	—	—	—	—	*	*	—	—	—
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← (ear)	—	—	—	—	—	*	*	—	—	—
MOVW io, #imm16	4	5	0	(c)	word (RWi) ← (eam)	—	—	—	—	—	*	*	—	—	—
MOVW ear, #imm16	4	2	1	0	word (ear) ← (RWi)	—	—	—	—	—	*	*	—	—	—
MOVW eam, #imm16	4+	4+ (a)	0	(c)	word (eam) ← (RWi)	—	—	—	—	—	—	—	—	—	—
					word (RWi) ← imm16						*	*	—	—	—
MOVW AL, AH	2	3	0	(c)	word (io) ← imm16	—	—	—	—	—	*	*	—	—	—
MOVW @A, T					word (ear) ← imm16										
					word (eam) ← imm16										
XCHW A, ear	2	4	2	0		—	—	—	—	—	—	—	—	—	—
XCHW A, eam	2+	5+ (a)	0	2× (c)	word ((A)) ← (AH)	—	—	—	—	—	—	—	—	—	—
XCHW RWi, ear	2	7	4	0		—	—	—	—	—	—	—	—	—	—
XCHW RWi, eam	2+	9+ (a)	2	2× (c)		—	—	—	—	—	—	—	—	—	—
					word (A) ↔ (ear)										
					word (A) ↔ (eam)										
					word (RWi) ↔ (ear)										
					word (RWi) ↔ (eam)										
MOVL A, ear	2	4	2	0	long (A) ← (ear)	—	—	—	—	—	*	*	—	—	—
MOVL A, eam	2+	5+ (a)	0	(d)	long (A) ← (eam)	—	—	—	—	—	*	*	—	—	—
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	—	—	—	—	—	*	*	—	—	—
MOVL ear, A	2	4	2	0	long (ear) ← (A)	—	—	—	—	—	*	*	—	—	—
MOVL eam, A	2+	5+ (a)	0	(d)	long (eam) ← (A)	—	—	—	—	—	*	*	—	—	—

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
ADD	2	2	0	0	byte (A) ← (A) +imm8	Z	—	—	—	—	*	*	*	*	—
A,#imm8	2	5	0	(b)	byte (A) ← (A) +(dir)	Z	—	—	—	—	*	*	*	*	—
ADD A, dir	2	3	1	0	byte (A) ← (A) +(ear)	Z	—	—	—	—	*	*	*	*	—
ADD A, ear	2+	4+ (a)	0	(b)	byte (A) ← (A) +(eam)	Z	—	—	—	—	*	*	*	*	—
ADD A, eam	2	3	2	0	byte (ear) ← (ear) + (A)	—	—	—	—	—	*	*	*	*	—
ADD ear, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) + (A)	Z	—	—	—	—	*	*	*	*	*
ADD eam, A	1	2	0	0	byte (A) ← (AH) + (AL) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDC A	2	3	1	0	byte (A) ← (A) + (ear) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDC A, ear	2+	4+ (a)	0	(b)	byte (A) ← (A) + (eam) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDC A, eam	1	3	0	0	byte (A) ← (AH) + (AL) + (C)	Z	—	—	—	—	*	*	*	*	—
ADDDC A	2	2	0	0	(decimal)	Z	—	—	—	—	*	*	*	*	—
SUB A,	2	5	0	(b)	byte (A) ← (A) -imm8	Z	—	—	—	—	*	*	*	*	—
#imm8	2	3	1	0	byte (A) ← (A) - (dir)	Z	—	—	—	—	*	*	*	*	—
SUB A, dir	2+	4+ (a)	0	(b)	byte (A) ← (A) - (ear)	Z	—	—	—	—	*	*	*	*	—
SUB A, ear	2	3	2	0	byte (A) ← (A) - (eam)	—	—	—	—	—	*	*	*	*	—
SUB A, eam	2+	5+ (a)	0	2× (b)	byte (ear) ← (ear) - (A)	—	—	—	—	—	*	*	*	*	*
SUB ear, A	1	2	0	0	byte (eam) ← (eam) - (A)	Z	—	—	—	—	*	*	*	*	—
SUB eam, A	2	3	1	0	byte (A) ← (AH) - (AL) - (C)	Z	—	—	—	—	*	*	*	*	—
SUBC A	2+	4+ (a)	0	(b)	byte (A) ← (A) - (ear) - (C)	Z	—	—	—	—	*	*	*	*	—
SUBC A, ear	1	3	0	0	byte (A) ← (A) - (eam) - (C)	Z	—	—	—	—	*	*	*	*	—
SUBC A, eam					byte (A) ← (AH) - (AL) - (C)						*	*	*	*	
SUBDC A					(decimal)						*	*	*	*	
ADDW A	1	2	0	0	word (A) ← (AH) + (AL)	—	—	—	—	—	*	*	*	*	—
ADDW A, ear	2	3	1	0	word (A) ← (A) +(ear)	—	—	—	—	—	*	*	*	*	—
ADDW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) +(eam)	—	—	—	—	—	*	*	*	*	—
ADDW A,	3	2	0	0	word (A) ← (A) +imm16	—	—	—	—	—	*	*	*	*	—
#imm16	2	3	2	0	word (ear) ← (ear) + (A)	—	—	—	—	—	*	*	*	*	—
ADDW ear, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) + (A)	—	—	—	—	—	*	*	*	*	*
ADDW eam, A	2	3	1	0	word (A) ← (A) + (ear) + (C)	—	—	—	—	—	*	*	*	*	—
ADDCW A, ear	2+	4+ (a)	0	(c)	word (A) ← (A) + (eam) + (C)	—	—	—	—	—	*	*	*	*	—
ADDCW A, eam	1	2	0	0	word (A) ← (AH) - (AL)	—	—	—	—	—	*	*	*	*	—
SUBW A	2	3	1	0	word (A) ← (A) - (ear)	—	—	—	—	—	*	*	*	*	—
SUBW A, ear	2+	4+ (a)	0	(c)	word (A) ← (A) - (eam)	—	—	—	—	—	*	*	*	*	—
SUBW A, eam	3	2	0	0	word (A) ← (A) -imm16	—	—	—	—	—	*	*	*	*	—
SUBW A,	2	3	2	0	word (ear) ← (ear) - (A)	—	—	—	—	—	*	*	*	*	—
#imm16	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) - (A)	—	—	—	—	—	*	*	*	*	*
SUBW ear, A	2	3	1	0	word (A) ← (A) - (ear) - (C)	—	—	—	—	—	*	*	*	*	—
SUBW eam, A	2+	4+ (a)	0	(c)	word (A) ← (A) - (eam) - (C)	—	—	—	—	—	*	*	*	*	—
SUBCW A, ear											*	*	*	*	
SUBCW A, eam											*	*	*	*	
ADDL A, ear	2	6	2	0	long (A) ← (A) + (ear)	—	—	—	—	—	*	*	*	*	—
ADDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) + (eam)	—	—	—	—	—	*	*	*	*	—
ADDL A,	5	4	0	0	long (A) ← (A) +imm32	—	—	—	—	—	*	*	*	*	—
#imm32	2	6	2	0	long (A) ← (A) - (ear)	—	—	—	—	—	*	*	*	*	—
SUBL A, ear	2+	7+ (a)	0	(d)	long (A) ← (A) - (eam)	—	—	—	—	—	*	*	*	*	—
SUBL A, eam	5	4	0	0	long (A) ← (A) -imm32	—	—	—	—	—	*	*	*	*	—
SUBL A,											*	*	*	*	
#imm32											*	*	*	*	

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
INC ear	2	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC ear	2	3	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DEC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW ear	2	3	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCW eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW ear	2	3	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECW eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL ear	2	7	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCL eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL ear	2	7	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECL eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
CMP A	1	1	0	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP A, ear	2	2	1	0	byte (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMP A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMP A, #imm8	2	2	0	0	byte (A) ← imm8	–	–	–	–	–	*	*	*	*	–
CMPW A	1	1	0	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW A, ear	2	2	1	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPW A, #imm16	3	2	0	0	word (A) ← imm16	–	–	–	–	–	*	*	*	*	–
CMPL A, ear	2	6	2	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPL A, eam	2+	7+ (a)	0	(d)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPL A, #imm32	5	3	0	0	word (A) ← imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 12 Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
DIVU A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder →	-	-	-	-	-	-	-	*	*	-
DIVU A, ear	2	*2	1	0	byte (AH) word (A)/byte (ear)	-	-	-	-	-	-	-	*	*	-
DIVU A, eam	2+	*3	0	*6	Quotient → byte (A) Remainder → byte (ear)	-	-	-	-	-	-	-	*	*	-
DIVUW A, ear	2	*4	1	0	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	-	-	-	-	-	-	-	*	*	-
DIVUW A, eam	2+	*5	0	*7	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	-	-	-	-	-	-	-	-	-	-
	2	*9	1	0	long (A)/word (eam)	-	-	-	-	-	-	-	-	-	-
	2+	*10	0	(b)	Quotient → word (A) Remainder → word (eam)	-	-	-	-	-	-	-	-	-	-
MULU A	1	*11	0	0		-	-	-	-	-	-	-	-	-	-
MULU A, ear	2	*12	1	0	byte (AH) *byte (AL) → word (A)	-	-	-	-	-	-	-	-	-	-
MULU A, eam	2+	*13	0	(c)	byte (A) *byte (ear) → word (A) byte (A) *byte (eam) → word (A)	-	-	-	-	-	-	-	-	-	-
MULUW A, MULUW A, ear MULUW A, eam					word (AH) *word (AL) → long (A) word (A) *word (ear) → long (A) word (A) *word (eam) → long (A)										

*1: 3 when the result is zero, 7 when an overflow occurs, and 15 normally.

*2: 4 when the result is zero, 8 when an overflow occurs, and 16 normally.

*3: 6 + (a) when the result is zero, 9 + (a) when an overflow occurs, and 19 + (a) normally.

*4: 4 when the result is zero, 7 when an overflow occurs, and 22 normally.

*5: 6 + (a) when the result is zero, 8 + (a) when an overflow occurs, and 26 + (a) normally.

*6: (b) when the result is zero or when an overflow occurs, and 2 × (b) normally.

*7: (c) when the result is zero or when an overflow occurs, and 2 × (c) normally.

*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not zero.

*9: 4 when byte (ear) is zero, and 8 when byte (ear) is not zero.

*10: 5 + (a) when byte (eam) is zero, and 9 + (a) when byte (eam) is not 0.

*11: 3 when word (AH) is zero, and 11 when word (AH) is not zero.

*12: 4 when word (ear) is zero, and 12 when word (ear) is not zero.

*13: 5 + (a) when word (eam) is zero, and 13 + (a) when word (eam) is not zero.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 13 Logical 1 Instructions (Byte/Word) [39 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
AND A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	—	—	—	—	—	*	*	R	—	—
AND A, ear	2	3	1	0	byte (A) ← (A) and (ear)	—	—	—	—	—	*	*	R	—	—
AND A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) and (eam)	—	—	—	—	—	*	*	R	—	—
AND ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	—	—	—	—	—	*	*	R	—	—
AND eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) and (A)	—	—	—	—	—	*	*	R	—	*
OR A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	—	—	—	—	—	*	*	R	—	—
OR A, ear	2	3	1	0	byte (A) ← (A) or (ear)	—	—	—	—	—	*	*	R	—	—
OR A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) or (eam)	—	—	—	—	—	*	*	R	—	—
OR ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	—	—	—	—	—	*	*	R	—	—
OR eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) or (A)	—	—	—	—	—	*	*	R	—	*
XOR A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	—	—	—	—	—	*	*	R	—	—
XOR A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	—	—	—	—	—	*	*	R	—	—
XOR A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) xor (eam)	—	—	—	—	—	*	*	R	—	—
XOR ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	—	—	—	—	—	*	*	R	—	—
XOR eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) xor (A)	—	—	—	—	—	*	*	R	—	*
NOT A	1	2	0	0	byte (A) ← not (A)	—	—	—	—	—	*	*	R	—	—
NOT ear	2	3	2	0	byte (ear) ← not (ear)	—	—	—	—	—	*	*	R	—	—
NOT eam	2+	5+ (a)	0	2× (b)	byte (eam) ← not (eam)	—	—	—	—	—	*	*	R	—	*
ANDW A	1	2	0	0	word (A) ← (AH) and (A)	—	—	—	—	—	*	*	R	—	—
ANDW A, #imm16	3	2	0	0	word (A) ← (A) and imm16	—	—	—	—	—	*	*	R	—	—
ANDW A, ear	2	3	1	0	word (A) ← (A) and (ear)	—	—	—	—	—	*	*	R	—	—
ANDW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) and (eam)	—	—	—	—	—	*	*	R	—	—
ANDW ear, A	2	3	2	0	word (ear) ← (ear) and (A)	—	—	—	—	—	*	*	R	—	—
ANDW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) and (A)	—	—	—	—	—	*	*	R	—	*
ORW A	1	2	0	0	word (A) ← (AH) or (A)	—	—	—	—	—	*	*	R	—	—
ORW A, #imm16	3	2	0	0	word (A) ← (A) or imm16	—	—	—	—	—	*	*	R	—	—
ORW A, ear	2	3	1	0	word (A) ← (A) or (ear)	—	—	—	—	—	*	*	R	—	—
ORW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) or (eam)	—	—	—	—	—	*	*	R	—	—
ORW ear, A	2	3	2	0	word (ear) ← (ear) or (A)	—	—	—	—	—	*	*	R	—	—
ORW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) or (A)	—	—	—	—	—	*	*	R	—	*
XORW A	1	2	0	0	word (A) ← (AH) xor (A)	—	—	—	—	—	*	*	R	—	—
XORW A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	—	—	—	—	—	*	*	R	—	—
XORW A, ear	2	3	1	0	word (A) ← (A) xor (ear)	—	—	—	—	—	*	*	R	—	—
XORW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) xor (eam)	—	—	—	—	—	*	*	R	—	—
XORW ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	—	—	—	—	—	*	*	R	—	—
XORW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) xor (A)	—	—	—	—	—	*	*	R	—	*
NOTW A	1	2	0	0	word (A) ← not (A)	—	—	—	—	—	*	*	R	—	—
NOTW ear	2	3	2	0	word (ear) ← not (ear)	—	—	—	—	—	*	*	R	—	—
NOTW eam	2+	5+ (a)	0	2× (c)	word (eam) ← not (eam)	—	—	—	—	—	*	*	R	—	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 14 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
ANDL A, ear	2	6	2	0	long (A) ← (A) and (ear)	-	-	-	-	-	*	*	R	-	-
ANDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) and (eam)	-	-	-	-	-	*	*	R	-	-
ORL A, ear	2	6	2	0	long (A) ← (A) or (ear)	-	-	-	-	-	*	*	R	-	-
ORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) or (eam)	-	-	-	-	-	*	*	R	-	-
XORL A, ea	2	6	2	0	long (A) ← (A) xor (ear)	-	-	-	-	-	*	*	R	-	-
XORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) xor (eam)	-	-	-	-	-	*	*	R	-	-

Table 15 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
NEG A	1	2	0	0	byte (A) ← 0 - (A)	X	-	-	-	-	*	*	*	*	-
NEG ear	2	3	2	0	byte (ear) ← 0 - (ear)	-	-	-	-	-	*	*	*	*	-
NEG eam	2+	5+ (a)	0	2× (b)	byte (eam) ← 0 - (eam)	-	-	-	-	-	*	*	*	*	*
NEGW A	1	2	0	0	word (A) ← 0 - (A)	-	-	-	-	-	*	*	*	*	-
NEGW ear	2	3	2	0	word (ear) ← 0 - (ear)	-	-	-	-	-	*	*	*	*	-
NEGW eam	2+	5+ (a)	0	2× (c)	word (eam) ← 0 - (eam)	-	-	-	-	-	*	*	*	*	*

Table 16 Normalize Instruction (Long Word) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
NRML A, R0	2	*1	1	0	long (A) ← Shift until first digit is "1" byte (R0) ← Current shift count	-	-	-	-	-	-	*	-	-	-

*1: 4 when the contents of the accumulator are all zeroes, 6 + (R0) in all other cases (shift count).

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

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Table 17 Shift Instructions (Byte/Word/Long Word) [18 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
RORCA	2	2	0	0	byte (A) ← Right rotation with carry	-	-	-	-	-	*	*	-	*	-
ROLCA	2	2	0	0	byte (A) ← Left rotation with carry	-	-	-	-	-	*	*	-	*	-
RORCear	2	3	2	0	byte (ear) ← Right rotation with carry	-	-	-	-	-	*	*	-	*	-
RORCeam	2+	5+	0	2× (b)	byte (eam) ← Right rotation with carry	-	-	-	-	-	*	*	-	*	*
ROLC ear	2	(a)	2	0	byte (ear) ← Left rotation with carry	-	-	-	-	-	*	*	-	*	-
ROLC eam	2+	3	0	2× (b)	byte (ear) ← Left rotation with carry	-	-	-	-	-	*	*	-	*	*
		5+			byte (eam) ← Left rotation with carry										
ASR A, R0	2	(a)	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-
LSR A, R0	2		1	0	byte (A) ← Logical right barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	-	-	-	-	-	*	*	-	*	-
		*1													
		*1													
ASRWA	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	-	-	-	-	*	*	*	-	*	-
LSRWA/SHRW	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	-	-	-	-	*	R	*	-	*	-
A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	-	-	-	-	*	*	*	-	*	-
LSLW A/SHLW	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-
A	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-
ASRWA, R0	2	*1	1	0	word (A) ← Logical left barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-
LSRWA, R0															
LSLW A, R0															
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right shift (A, R0)	-	-	-	-	*	*	*	-	*	-
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	-	-	-	-	*	*	*	-	*	-

*1: 6 when R0 is 0, 5 + (R0) in all other cases.

*2: 6 when R0 is 0, 6 + (R0) in all other cases.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 18 Branch 1 Instructions [31 Instructions]

Mnemonic	#	~	RG	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
BZ/BEQ	rel	2	*1	0	0	Branch when (Z) = 1	-	-	-	-	-	-	-	-	-
BNZ/BNE	rel	2	*1	0	0	Branch when (Z) = 0	-	-	-	-	-	-	-	-	-
BC/BLO	rel	2	*1	0	0	Branch when (C) = 1	-	-	-	-	-	-	-	-	-
BNC/BHS	rel	2	*1	0	0	Branch when (C) = 0	-	-	-	-	-	-	-	-	-
BN	rel	2	*1	0	0	Branch when (N) = 1	-	-	-	-	-	-	-	-	-
BP	rel	2	*1	0	0	Branch when (N) = 0	-	-	-	-	-	-	-	-	-
BV	rel	2	*1	0	0	Branch when (V) = 1	-	-	-	-	-	-	-	-	-
BNV	rel	2	*1	0	0	Branch when (V) = 0	-	-	-	-	-	-	-	-	-
BT	rel	2	*1	0	0	Branch when (T) = 1	-	-	-	-	-	-	-	-	-
BNT	rel	2	*1	0	0	Branch when (T) = 0	-	-	-	-	-	-	-	-	-
BLT	rel	2	*1	0	0	Branch when (V) xor (N) = 1	-	-	-	-	-	-	-	-	-
BGE	rel	2	*1	0	0	Branch when (V) xor (N) = 0	-	-	-	-	-	-	-	-	-
BLE	rel	2	*1	0	0	Branch when ((V) xor (N)) or	-	-	-	-	-	-	-	-	-
BGT	rel	2	*1	0	0	(Z) = 1	-	-	-	-	-	-	-	-	-
BLS	rel	2	*1	0	0	Branch when ((V) xor (N)) or	-	-	-	-	-	-	-	-	-
BHI	rel	2	*1	0	0	(Z) = 0	-	-	-	-	-	-	-	-	-
BRA	rel	2	*1	0	0	Branch when (C) or (Z) = 1	-	-	-	-	-	-	-	-	-
						Branch when (C) or (Z) = 0	-	-	-	-	-	-	-	-	-
JMP	@A	1	2	0	0	Branch unconditionally	-	-	-	-	-	-	-	-	-
JMP	addr16	3	3	0	0		-	-	-	-	-	-	-	-	-
JMP	@ear	2	3	1	0	word (PC) ← (A)	-	-	-	-	-	-	-	-	-
JMP	@eam	2+	4+ (a)	0	(c)	word (PC) ← addr16	-	-	-	-	-	-	-	-	-
JMPP	@ear *3	2	5	2	0	word (PC) ← (ear)	-	-	-	-	-	-	-	-	-
JMPP	@eam *3	2+	6+ (a)	0	(d)	word (PC) ← (eam)	-	-	-	-	-	-	-	-	-
JMPP	addr24	4	4	0	0	word (PC) ← (ear), (PCB) ← (ear +2)	-	-	-	-	-	-	-	-	-
CALL	@ear *4	2	6	1	(c)	word (PC) ← (eam), (PCB) ←	-	-	-	-	-	-	-	-	-
CALL	@eam *4	2+	7+ (a)	0	2× (c)	(eam +2)	-	-	-	-	-	-	-	-	-
CALL	addr16 *5	3	6	0	(c)	word (PC) ← ad24 0 to 15,	-	-	-	-	-	-	-	-	-
CALLV	#vct4 *5	1	7	0	2× (c)	(PCB) ← ad24 16 to 23	-	-	-	-	-	-	-	-	-
CALLP	@ear *6	2	10	2	2× (c)	word (PC) ← (ear)	-	-	-	-	-	-	-	-	-
						word (PC) ← (eam)	-	-	-	-	-	-	-	-	-
CALLP	@eam *6	2+	11+ (a)	0	*2	word (PC) ← addr16	-	-	-	-	-	-	-	-	-
						Vector call instruction	-	-	-	-	-	-	-	-	-
CALLP	addr24 *7	4	10	0	2× (c)	word (PC) ← (ear) 0 to 15 (PCB) ← (ear) 16 to 23 word (PC) ← (eam) 0 to 15 (PCB) ← (eam) 16 to 23 word (PC) ← addr0 to 15, (PCB) ← addr16 to 23	-	-	-	-	-	-	-	-	-

*1: 4 when branching, 3 when not branching.

*2: (b) + 3 × (c)

*3: Read (word) branch address.

*4: W: Save (word) to stack; R: read (word) branch address.

*5: Save (word) to stack.

*6: W: Save (long word) to W stack; R: read (long word) R branch address.

*7: Save (long word) to stack.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 19 Branch 2 Instructions [19 Instructions]

Mnemonic	#	~	RG	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
CBNE A, #imm8, rel	3	*1	0	0	Branch when byte (A) ≠ imm8	—	—	—	—	—	*	*	*	*	—
CWBNEA, #imm16, rel	4	*1	0	0	Branch when word (A) ≠ imm16	—	—	—	—	—	*	*	*	*	—
CBNE ear, #imm8, rel	4	*2	1	0	Branch when byte (ear) ≠ imm8	—	—	—	—	—	*	*	*	*	—
CBNE eam, #imm8, rel ^{*9}	4+	*3	0	(b)											
CWBNEear, #imm16, rel	5	*4	1	0	Branch when byte (eam) ≠ imm8	—	—	—	—	—	*	*	*	*	—
CWBNEeam, #imm16, rel ^{*9}	5+	*3	0	(c)											
DBNZ ear, rel	3+	*6	2	2× (b)	Branch when word (ear) ≠ imm16	—	—	—	—	—	*	*	*	—	*
DBNZ eam, rel	3	*5	2	0	Branch when word (eam) ≠ imm16	—	—	—	—	—	*	*	*	—	—
DWBNZ ear, rel	3+	*6	2	2× (c)											
DWBNZ eam, rel	2	20	0	8× (c)	Branch when byte (ear) = (ear) - 1, and (ear) ≠ 0	—	—	R	S	—	—	—	—	—	—
INT #vct8 INT addr16 INTP addr24	3	16	0	6× (c)	Branch when byte (eam) = (eam) - 1, and (eam) ≠ 0	—	—	R	S	—	—	—	—	—	—
	4	17	0	6× (c)	Branch when word (ear) = (ear) - 1, and (ear) ≠ 0	—	—	R	S	—	—	—	—	—	—
	1	20	0	8× (c)	Branch when word (eam) = (eam) - 1, and (eam) ≠ 0	—	—	R	S	—	—	—	—	—	—
INT9 RETI	1	15	0	6× (c)	Branch when word (eam) = (eam) - 1, and (eam) ≠ 0	—	—	*	*	*	*	*	*	*	—
LINK #local8	2	6	0	(c)	Software interrupt	—	—	—	—	—	—	—	—	—	—
UNLINK	1	4	0	(c)	Software interrupt	—	—	—	—	—	—	—	—	—	—
	1	6	0	(d)	Software interrupt	—	—	—	—	—	—	—	—	—	—
RET ^{*7} RETP ^{*8}	1	5	0	(c)	Return from interrupt	—	—	—	—	—	—	—	—	—	—
					At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	—	—	—	—	—	—	—	—	—	—
					At constant entry, retrieve old frame pointer from stack.	—	—	—	—	—	—	—	—	—	—
					Return from subroutine	—	—	—	—	—	—	—	—	—	—
					Return from subroutine	—	—	—	—	—	—	—	—	—	—

*1: 5 when branching, 4 when not branching

*2: 13 when branching, 12 when not branching

*3: 7 + (a) when branching, 6 + (a) when not branching

*4: 8 when branching, 7 when not branching

*5: 7 when branching, 6 when not branching

*6: 8 + (a) when branching, 7 + (a) when not branching

*7: Retrieve (word) from stack

*8: Retrieve (long word) from stack

*9: In the CBNE/CWBNE instruction, do not use the RWj+ addressing mode.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 20 Other Control Instructions (Byte/Word/Long Word) [28 Instructions]

Mnemonic	#	~	RG	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
PUSHWA	1	4	0	(c)	word (SP) ← (SP) -2, ((SP)) ←	-	-	-	-	-	-	-	-	-	-
PUSHWAH	1	4	0	(c)	(A)	-	-	-	-	-	-	-	-	-	-
PUSHWPS	1	4	0	(c)	word (SP) ← (SP) -2, ((SP)) ←	-	-	-	-	-	-	-	-	-	-
PUSHWr1st	2	*3	*5	*4	(AH)	-	-	-	-	-	-	-	-	-	-
					word (SP) ← (SP) -2, ((SP)) ←	-	-	-	-	-	-	-	-	-	-
POPW A	1	3	0	(c)	(PS)	-	*	-	-	-	-	-	-	-	-
POPW AH	1	3	0	(c)	(SP) ← (SP) -2n, ((SP)) ←	-	-	-	-	-	-	-	-	-	-
POPW PS	1	4	0	(c)	(r1st)	-	-	*	*	*	*	*	*	*	-
POPW r1st	2	*2	*5	*4		-	-	-	-	-	-	-	-	-	-
JCTX @A	1	14	0	6× (c)	word (A) ← ((SP)), (SP) ← (SP) +2	-	-	*	*	*	*	*	*	*	-
AND CCR, #imm8	2	3	0	0	word (AH) ← ((SP)), (SP) ← (SP) +2	-	-	*	*	*	*	*	*	*	-
OR CCR, #imm8	2	3	0	0	word (PS) ← ((SP)), (SP) ← (SP) +2	-	-	*	*	*	*	*	*	*	-
	2	2	0	0	(r1st) ← ((SP)), (SP) ← (SP) +2n	-	-	-	-	-	-	-	-	-	-
	2	2	0	0		-	-	-	-	-	-	-	-	-	-
MOV RP, #imm8	2	3	1	0	Context switch instruction	-	-	-	-	-	-	-	-	-	-
MOV ILM, #imm8	2+	2+ (a)	1	0		-	-	-	-	-	-	-	-	-	-
MOVEA RWi, ear	2	1	0	0	byte (CCR) ← (CCR) and imm8	-	*	-	-	-	-	-	-	-	-
MOVEA RWi, eam	2+	1+ (a)	0	0	byte (CCR) ← (CCR) or imm8	-	*	-	-	-	-	-	-	-	-
MOVEA A, ear	2	3	0	0	byte (RP) ←imm8	-	-	-	-	-	-	-	-	-	-
MOVEA A, eam	3	3	0	0	byte (ILM) ←imm8	-	-	-	-	-	-	-	-	-	-
ADDSP #imm8	2	*1	0	0	word (RWi) ←ear	Z	*	-	-	-	*	*	-	-	-
ADDSP #imm16	2	1	0	0	word (RWi) ←eam	-	-	-	-	-	*	*	-	-	-
MOV A, brgl	1	1	0	0	word(A) ←ear	-	-	-	-	-	-	-	-	-	-
MOV brg2, A	1	1	0	0	word (A) ←eam	-	-	-	-	-	-	-	-	-	-
	1	1	0	0		-	-	-	-	-	-	-	-	-	-
NOP	1	1	0	0	word (SP) ← (SP) +ext (imm8)	-	-	-	-	-	-	-	-	-	-
ADB	1	1	0	0	word (SP) ← (SP) +imm16	-	-	-	-	-	-	-	-	-	-
DTB	1	1	0	0		-	-	-	-	-	-	-	-	-	-
PCB	1	1	0	0	byte (A) ← (brgl)	-	-	-	-	-	-	-	-	-	-
SPB	1	1	0	0	byte (brg2) ← (A)	-	-	-	-	-	-	-	-	-	-
NCC					No operation										
CMR					Prefix code for accessing AD space										
					Prefix code for accessing DT space										
					Prefix code for accessing PC space										
					Prefix code for accessing SP space										
					Prefix code for no flag change										
					Prefix code for common register bank										

*1: PCB, ADB, SSB, USB, and SPB : 1 state

DTB, DPR : 2 states

*2: 7 + 3 × (pop count) + 2 × (last register number to be popped), 7 when r1st = 0 (no transfer register)

*3: 29 + (push count) - 3 × (last register number to be pushed), 8 when r1st = 0 (no transfer register)

*4: Pop count × (c), or push count × (c)

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*5: Pop count or push count.

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 21 Bit Manipulation Instructions [21 Instructions]

Mnemonic	#	~	RG	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
MOVB A, dir:bp	3	5	0	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB A, addr16:bp	4	5	0	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB A, io:bp	3	4	0	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB io:bp, A	3	6	0	2× (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
MOVB addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
MOVB io:bp, A	3	7	0	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB io:bp	3	7	0	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB io:bp	3	7	0	2× (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB dir:bp	4	*1	0	(b)	Branch when (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
CLRB addr16:bp	5	*1	0	(b)	Branch when (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
CLRB io:bp	4	*2	0	(b)	Branch when (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBC addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBC io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS dir:bp, rel	5	*3	0	2× (b)	Branch when (dir:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
BBS addr16:bp, rel	5	*3	0	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
BBS io:bp, rel	3	*4	0	*5	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
SBBS addr16:bp, rel	3	*4	0	*5	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–
WBTS io:bp															
WBTC io:bp															

*1: 8 when branching, 7 when not branching

*2: 7 when branching, 6 when not branching

*3: 10 when condition is satisfied, 9 when not satisfied

*4: Undefined count

*5: Until condition is satisfied

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 22 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
SWAP	1	3	0	0	byte (A) 0 to 7 ↔ (A) 8 to 15	-	-	-	-	-	-	-	-	-	-
SWAPW/XCHW AL, AH	1	2	0	0	word (AH) ↔ (AL)	-	*	-	-	-	-	-	-	-	-
EXT	1	1	0	0	byte sign extension	X	-	-	-	-	*	*	-	-	-
EXTW	1	2	0	0	word sign extension	-	X	-	-	-	*	*	-	-	-
ZEXT	1	1	0	0	byte zero extension	Z	-	-	-	-	R	*	-	-	-
ZEXTW	1	1	0	0	word zero extension	-	Z	-	-	-	R	*	-	-	-

Table 23 String Instructions [10 Instructions]

Mnemonic	#	~	R G	B	Operation	L H	A H	I	S	T	N	Z	V	C	RM W
MOVS/MOVS	2	*2	*5	*3	Byte transfer @AH+ ← @AL+, counter = RW0	-	-	-	-	-	-	-	-	-	-
MOVSD	2	*2	*5	*3	Byte transfer @AH- ← @AL-, counter = RW0	-	-	-	-	-	-	-	-	-	-
SCEQ/SCEQI	2	*1	*5	*4	Byte retrieval (@AH+) – AL, counter = RW0 Byte retrieval (@AH-) – AL, counter = RW0	-	-	-	-	-	*	*	*	*	-
SCEQD	2	*1	*5	*4		-	-	-	-	-	*	*	*	*	-
FISL/FILSI	2	6m +6	*5	*3	Byte filling @AH+ ← AL, counter = RW0	-	-	-	-	-	*	*	-	-	-
MOVSW/MOVSWI	2	*2	*8	*6	Word transfer @AH+ ← @AL+, counter = RW0 Word transfer @AH- ← @AL-, counter = RW0	-	-	-	-	-	-	-	-	-	-
MOVSWD	2	*2	*8	*6		-	-	-	-	-	-	-	-	-	-
SCWEQ/SCWEQI	2	*1	*8	*7	Word retrieval (@AH+) – AL, counter = RW0 Word retrieval (@AH-) – AL, counter = RW0	-	-	-	-	-	*	*	*	*	-
SCWEQD	2	*1	*8	*7		-	-	-	-	-	*	*	-	-	-
FILSW/FILSWI	2	6m +6	*8	*6	Word filling @AH+ ← AL, counter = RW0	-	-	-	-	-	*	*	-	-	-

m: RW0 value (counter value)

n: Loop count

*1: 5 when RW0 is 0, 4 + 7 × (RW0) for count out, and 7 × n + 5 when match occurs

*2: 5 when RW0 is 0, 4 + 8 × (RW0) in any other case

*3: (b) × (RW0) + (b) × (RW0) when accessing different areas for the source and destination, calculate (b) separately for each.

*4: (b) × n

*5: 2 × (RW0)

*6: (c) × (RW0) + (c) × (RW0) when accessing different areas for the source and destination, calculate (c) separately for each.

*7: (c) × n

*8: 2 × (RW0)

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

MB90670/675 Series

■ MASK OPTIONS

• MB90670 series

No.	Part number	MB90671 MB90672 MB90673	MB90P673	MB90V670
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P67, P70 to P77, P80, \overline{RST} , MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor
2	Pull-down resistors MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor

• MB90675 series

No.	Part number	MB90676 MB90677 MB90678	MB90P678	MB90V670
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P67, P70 to P77, P80 to P86, P90, P91, PA0 to PA7, PB0 to PB2, \overline{RST} , MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor
2	Pull-down resistors MD1, MD0	Specify by pin	Specify by pin	Without pull-up resistor

- Notes:
- The pull-up register configured as a port pin is switched-off in the stop mode and during the hardware standby.
 - In turning on power, option settings can not be made until clocks are supplied because 8 machine cycles are needed for option settings for the MB90P670/P675.

MB90670/675 Series

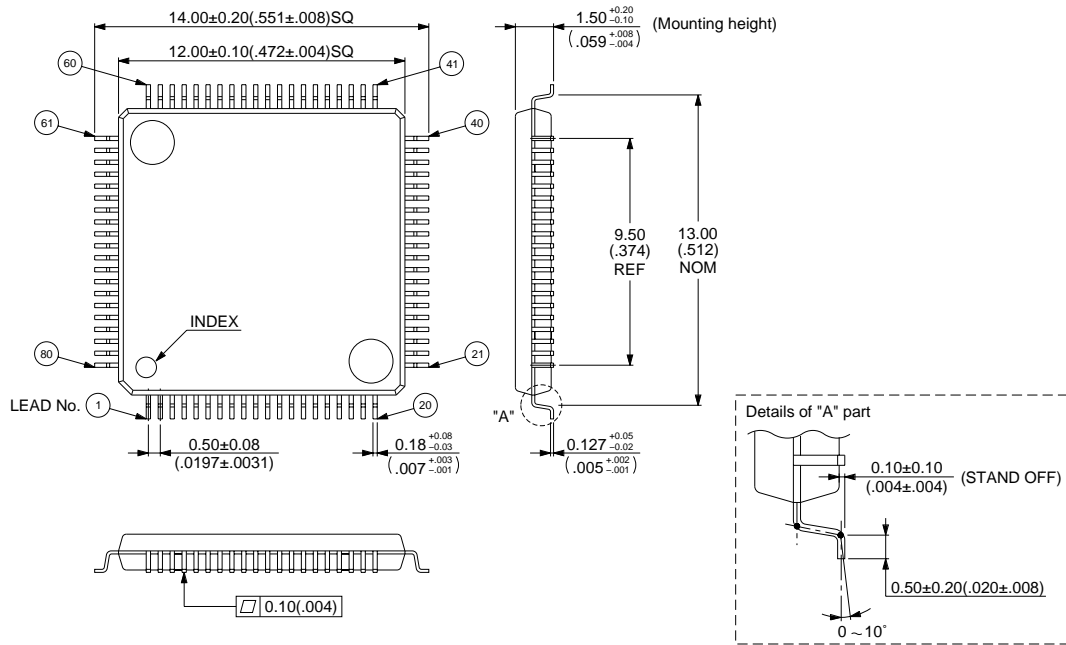
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90671PFV MB90672PFV MB90673PFV MB90T673PFV MB90P673PFV	80-pin Plastic LQFP (FPT-80P-M05)	
MB90671PF MB90672PF MB90673PF MB90T673PF MB90P673PF	80-pin Plastic QFP (FPT-80P-M06)	
MB90676PFV MB90677PFV MB90678PFV MB90T678PFV MB90P678PFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB90676PF MB90677PF MB90678PF MB90T678PF MB90P678PF	100-pin Plastic QFP (FPT-100P-M06)	

MB90670/675 Series

■ PACKAGE DIMENSIONS

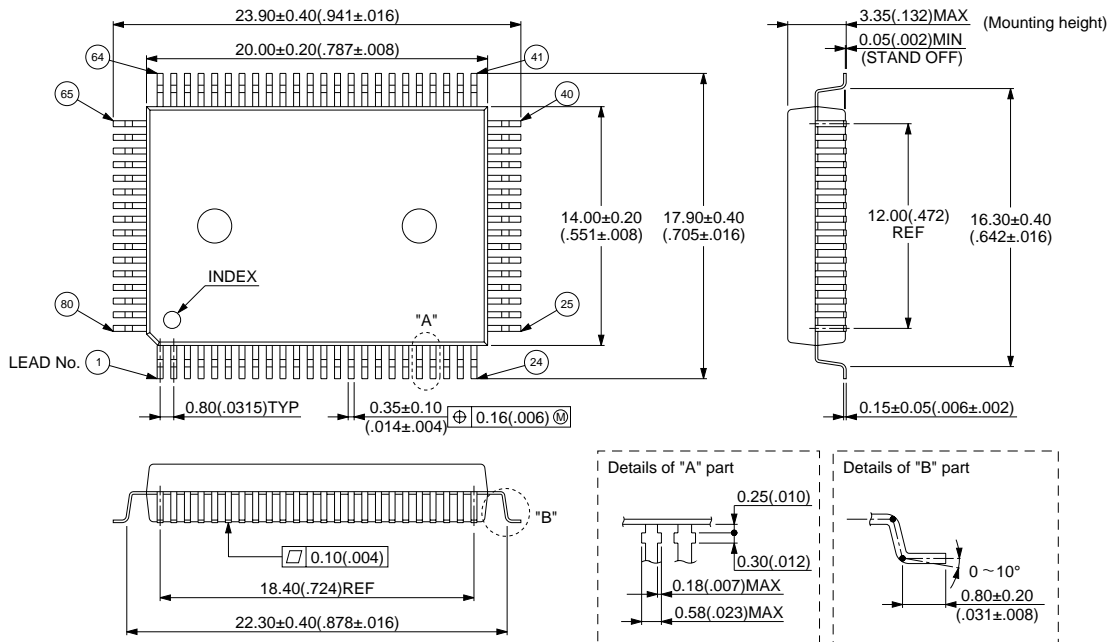
80-pin Plastic LQFP
(FPT-80P-M05)



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Dimensions in mm (inches)

80-pin Plastic QFP
(FPT-80P-M06)

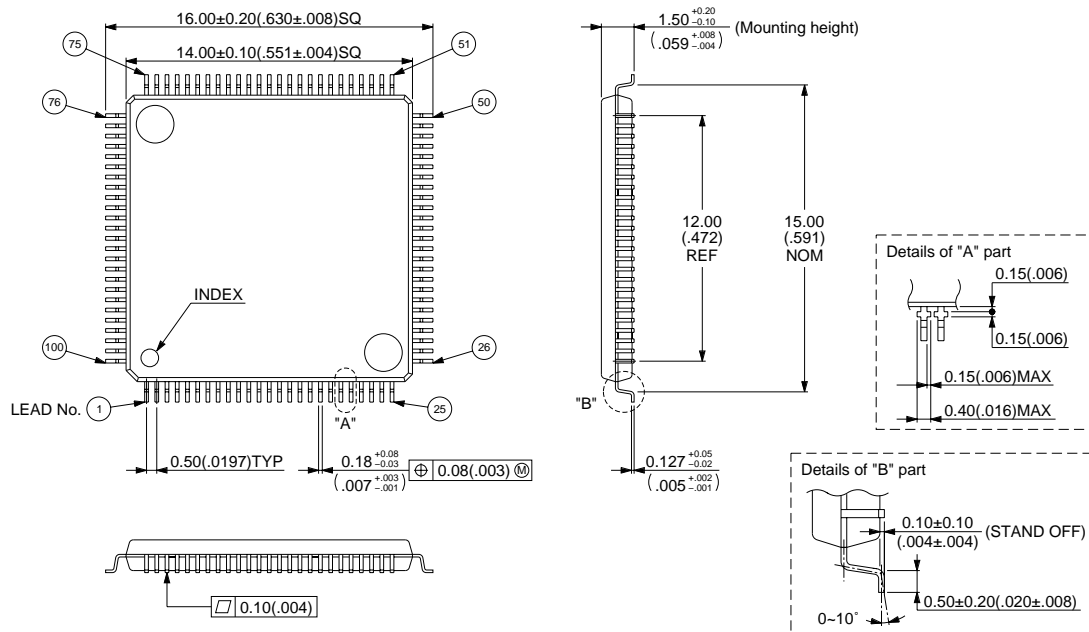


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Dimensions in mm (inches)

MB90670/675 Series

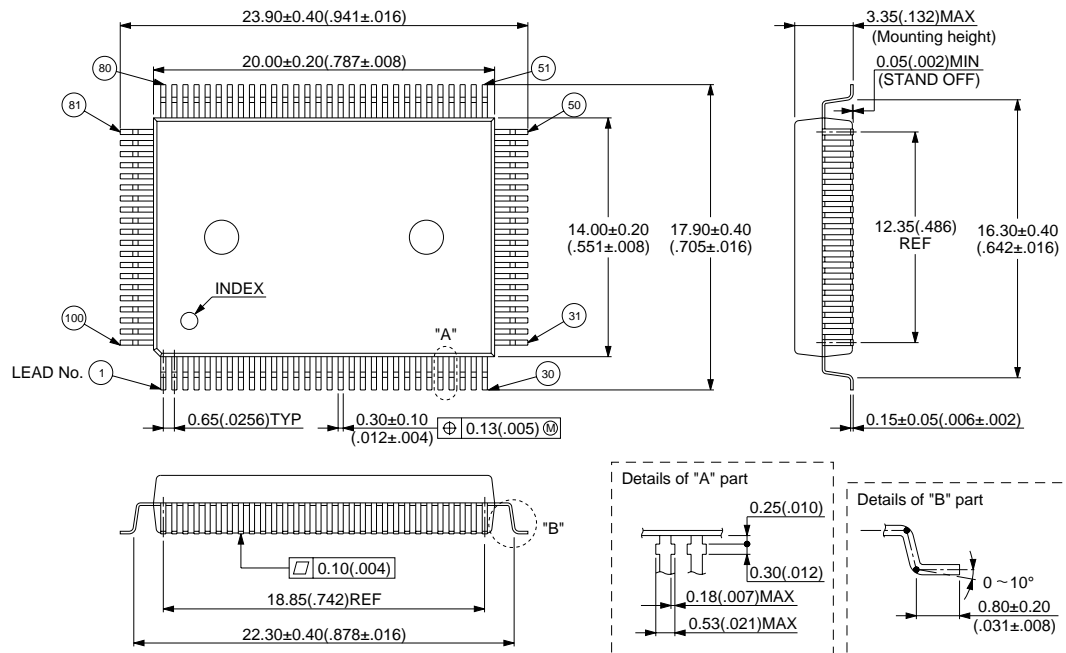
100-pin Plastic LQFP (FPT-100P-M05)



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Dimensions in mm (inches)

100-pin Plastic QFP (FPT-100P-M06)



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Dimensions in mm (inches)

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